



3C 5000L

J% &

自主决定命运, 创新成就未来



2010



Loongson Technology Corporation Limited

2

Building No.2, Loongson Industrial Park,
Zhongguancun Environmental Protection Park, Haidian District, Beijing
(Tel) 010-62546668
(Fax) 010-62600826



' 7) \$\$\$@

' 7) \$\$\$@



		3C5000L
		V1.2
%	J% \$	
&	J% %	
'	J% &	% ' <H

. gYfj] W4' ccb[gcb" Wb



1	1
1.1	1
1.2	3C5000L	2
2	5
2.1	5
2.2	5
3	7
3.1	7
3.2	8
3.3	9
4	17
4.1	0x0000	17
4.2	0x0008	17
4.3	0x0010	18
4.4	0x0020	18
4.5	0x0180	18
4.6	0x0188	19
4.7	0x0190	19
4.8	0x0198	20
4.9	0x01B0	20
4.10	0x01D0	23
4.11	0x01D8	23
4.12	0x0400	24
4.13	0x0420	24
4.14	0x0428	26
4.15	SRAM 0x0430	26
4.16	FUSE0 0x0460	26
4.17	FUSE1 0x0470	27
5	28



5.1

.....28.... ..

11 I/O	56
11.1 I/O	56
11.1.1	58
11.1.2	59
11.2 I/O	59
11.2.1	60
11.2.2	63
11.2.3 IO	63
11.2.4 IO HT	64
12	65
12.1	65
12.2	65
12.3	67
12.4	68
12.5	69
13 DDR4 SDRAM	71
13.1 DDR4 SDRAM	71
13.2 DDR4 SDRAM	72
13.3 DDR4 SDRAM	72
13.4 DDR4 SDRAM	72
13.4.1	72
13.5	84
13.5.1	84
13.5.2	84
13.5.3 Leveling	86
13.5.4	88
13.5.5 MRS	88
13.5.6	89
13.5.7	89
13.5.8 ECC	90
13.5.9	90

14	HyperTransport	94
14.1	HyperTransport	94
14.2	HyperTransport	96
14.3	HyperTransport	97
14.3.1	PIC	97
14.3.2		98
14.3.3		98
14.4	HyperTransport	99
14.4.1	HyperTransport	99
14.4.2	HyperTransport	99
14.5		100
14.5.1	Bridge Control	104
14.5.2	Capability Registers	105
14.5.3	Error Retry	107
14.5.4	Retry Count	108
14.5.5	Revision ID	108
14.5.6	Interrupt Discovery & Configuration	108
14.5.7		110
14.5.8		113
14.5.9	Link Train	115
14.5.10		116
14.5.11		120
14.5.12	POST	121
14.5.13		122
14.5.14	UNCACHE	123
14.5.15	P2P	126
14.5.16		128
14.5.17		130
14.5.18	PHY	131
14.5.19		131
14.5.20		132



14.5.21	132
14.5.22	133
14.5.23 Training 0	134
14.5.24 Training 0	134
14.5.25 Training 1	135
14.5.26 Training 2	135
14.5.27 Training 3	135
14.5.28)	



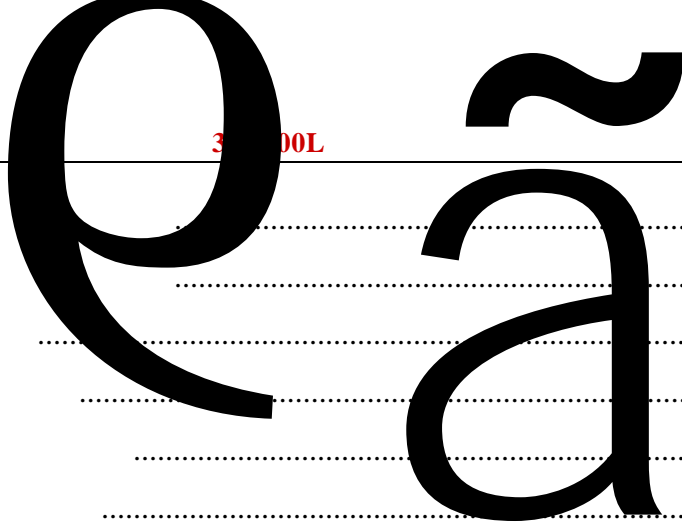
15.2.2	SPSR	155
15.2.3	TxFIFO	155
15.2.4	SPER	156
15.2.5	SFC_PARAM	156
15.2.6	SFC_SOFTCS	157
15.2.7	SFC_TIMING	157
15.2.8	CTRL	158
15.2.9	CMD	158
15.2.10	0 BUFO	158
15.2.11	1 BUF1	159
15.2.12	0 TIMERO	159
15.2.13	1 TIMER1	159
15.2.14	2 TIMER2	159
15.2.15	SPI	160
15.3	I2C	161
15.3.1	PRERlo	161
15.3.2	PRERhi	161
15.3.3	CTR	162
15.3.4	TXR	162
15.3.5	RXR	163
15.3.6	CR	163
15.3.7	SR	163
15.3.8	SLV_CTRL	164

2- 1	5
3- 1	7
3- 2	8
3- 3 SCID_SEL	8
3- 4 44	9
3- 5 MMAP	9
3- 6	10
3- 7MMAP	15
3- 8	15
3- 9 MMAP	16
4- 1	17
4- 2	17
4- 3	18
4- 4	18
4- 5	18
4- 6	19
4- 7	19
4- 8	20
4- 9	21
4- 10	22
4- 11	23
4- 12	23
4- 13	24
4- 14	24
4- 15	26
4- 16 SRAM	26
4- 17 FUSE	26
4- 18 FUSE	27

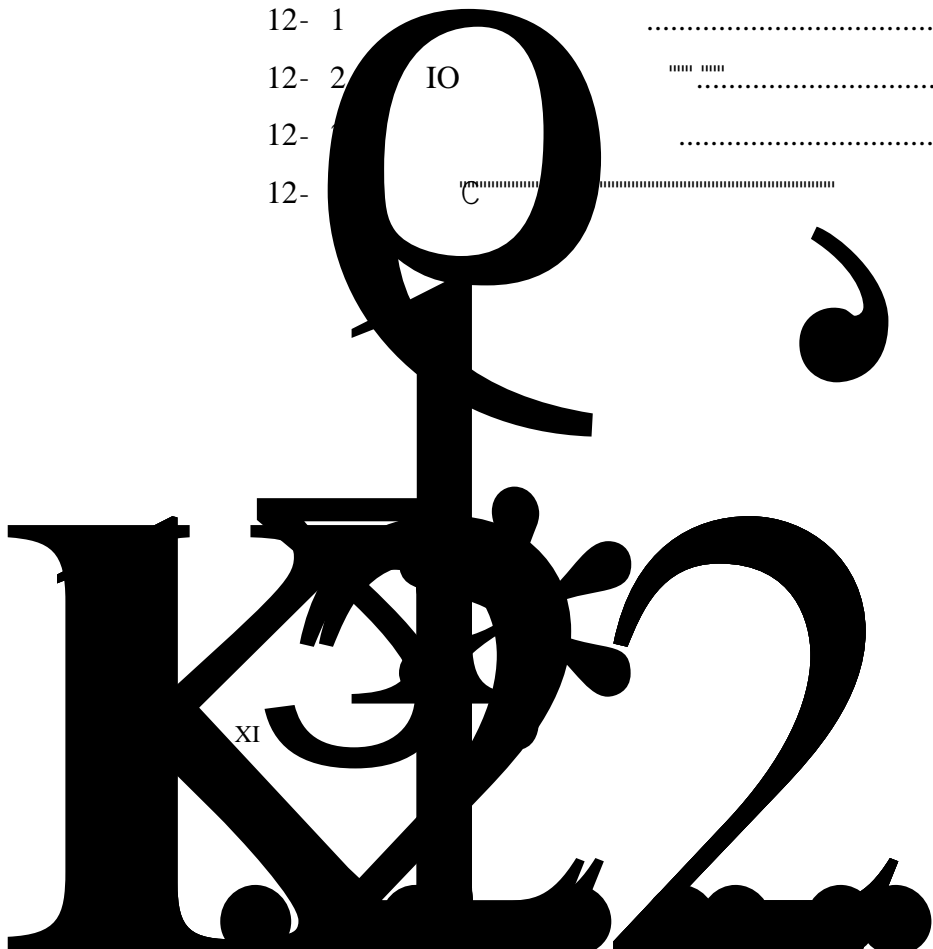
5- 1	28
5- 2	29
5- 3	29
5- 4	30
5- 5	30
5- 6	31
5- 7	31
5- 8	32
5- 9	32
5- 10	33
5- 11	33
5- 12 GPIO	34
6- 1	35
6- 2	36
6- 3	36
6- 4	36
6- 5 Node counter	38
7- 1	39
7- 2	39
7- 3	39
7- 4 GPIO	40
7- 5	41
8- 1 ' 7) \$\$\$@	44
9- 1 Cache	48
10- 1	51
10- 2 0	51
10- 3 1	52
10- 4 2	52
10- 5 3	52
10- 6	53



3 00L



10- 7		53
10- 8		55
11- 1		57
11- 2	IO	58
11- 3		58
11- 4		58
11- 5		59
11- 6		60
11- 7	IO	60
11- 8	IO	60
11- 9	IO	60
11- 10	IO	61
11- 11		61
11- 12		62
11- 13		62
11- 14		62
11- 15		63
11- 16	IO	63
11- 17	IO	63
12- 1		65
12- 2	IO	65
12- 3		66
12- 4	C	



XI



14- 2	HyperTransport	96
14- 3		97
14- 4		98
14- 5	4 HyperTransport	99
14- 6	3 HyperTransport	99
14- 7	3C5000L HyperTransport	99
14- 8	Bus Reset Control	104
14- 9	Command Capabilities Pointer Capability ID	105
14- 10	Link Config Link Control	105
14- 11	Revision ID Link Freq Link Error Link Freq Cap	106
14- 12	Feature Capability	107
14- 13	Error Retry	107
14- 14	Retry Count	108
14- 15	Revision ID	108
14- 16	Interrupt Capability	109
14- 17	Dataport	109
14- 18	IntrInfo 1	109
14- 19	IntrInfo 2	109
14- 20	HT 1	111
14- 21	HT 2	111
14- 22	HT 3	111
14- 23	HT 4	112
14- 24	HT 6	112
14- 25	HT 7	112
14- 26	HT 8	113
14- 27	HT 1	114
14- 28	HT 2	114
14- 29	HT 3	114
14- 30	HT 4	114
14- 31	HT 5	115

Λ

3C5000L

WV

3C200



14-	92 HT TX POST ID WIN1	141
14-	93 HT TX POST ID WIN2	141
14-	94 HT TX POST ID WIN3	142
14-	95 HT RX INT TRANS LO	142
14-	96 HT RX INT TRANS Hi	142
15-	1 SPI	154

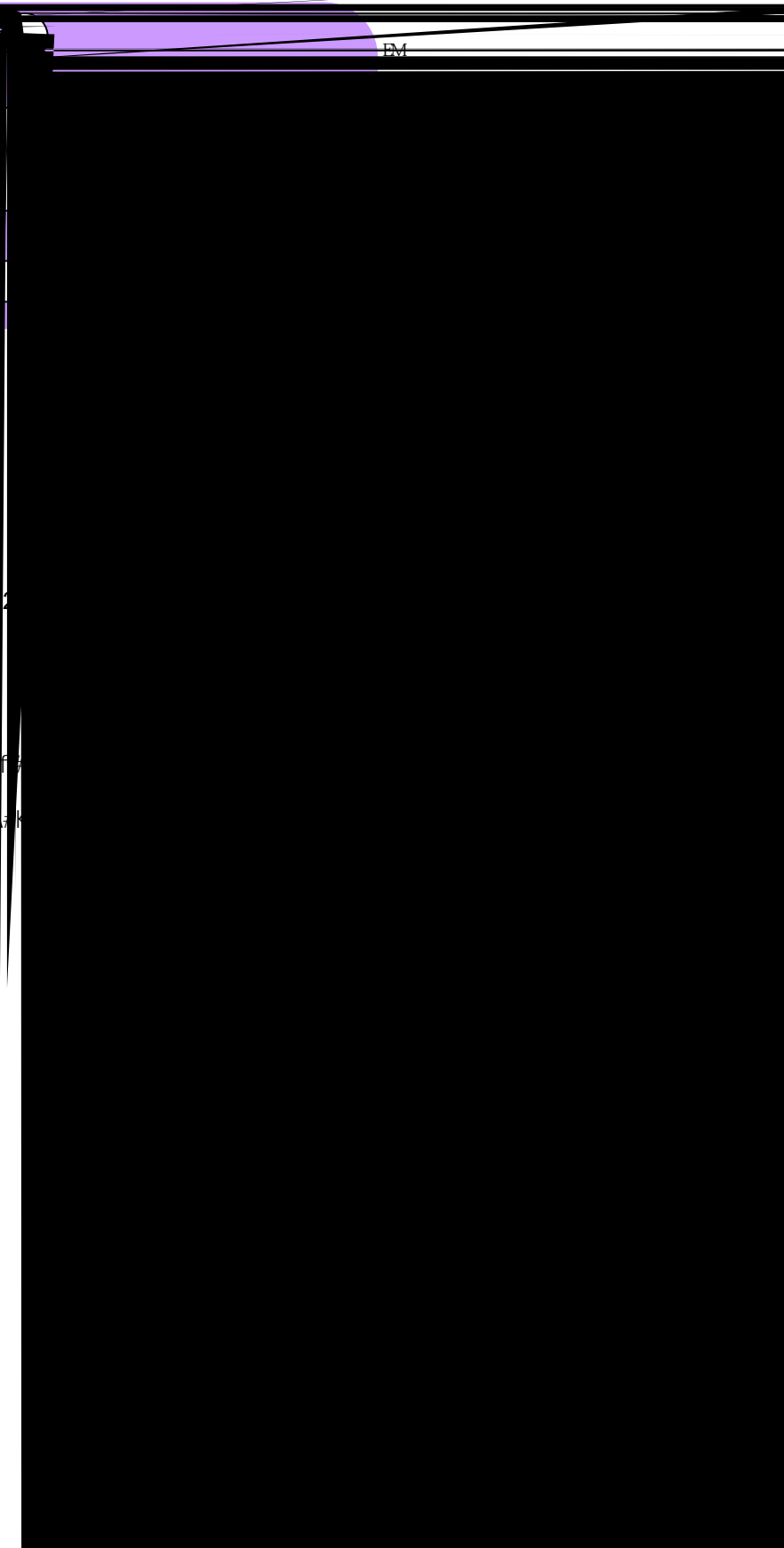
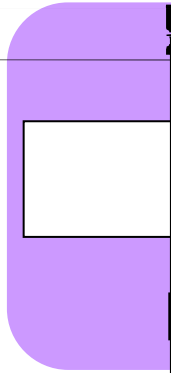


3C5000L



3C5000L

	'	% &	5L=	
7UWXY	=C		5L=	L% Gk] hW L%
	7UWXY		L& Gk] hW	L& 7UWXY



1- 2

, t, L%

D\$ D% D& D' G Uj Y

G\$ G% G& G' AUghYf #

=C 9A#9G GA#GG KA#K

L& AUghYf

G Uj Y

L% L&

1.2 3C5000L

' 7) \$\$\$@ ' 5) \$\$\$

&" \$; <n ! &" & <n



3C5000L

```
'      %*  *(          @5(*(
'      \      @CDC4&" $; <n
'      *(A6          7UWXY
'      =#C 8A5          7UWXY
'      (  +&  88F(          88F(!' &$ $
'      =C      (  <mYfHfUbgdcf h          <H          '" & <n
'      '      =&7 %  I 5FH %  GD= %*  ; D=C          "
```

d





2



MEM

1/2

7@G9@ . &Q

& V\$\$ (**A<n

& V\$% *\$\$A<n

& V/\$ G9

3

(, (

%* ((

' 7) \$\$\$@ (

3.1

(' 7) \$\$\$@ &#(77! BI A5

%* (

3- 1

		α+. ((0		
0	0	0	0x0000_0000_0000	0x0FFF_FFFF_FFFF
	1	1	0x1000_0000_0000	0x1FFF_FFFF_FFFF
	2	2	0x2000_0000_0000	0x2FFF_FFFF_FFFF
	3	3	0x3000_0000_0000	0x3FFF_FFFF_FFFF
1	4	4	0x4000_0000_0000	0x4FFF_FFFF_FFFF
	5	5	0x5000_0000_0000	0x5FFF_FFFF_FFFF
	6	6	0x6000_0000_0000	0x6FFF_FFFF_FFFF
	7	7	0x7000_0000_0000	0x7FFF_FFFF_FFFF
2	8	8	0x8000_0000_0000	0x8FFF_FFFF_FFFF
	9	9	0x9000_0000_0000	0x9FFF_FFFF_FFFF
	10	10	0xA000_0000_0000	0xAFFF_FFFF_FFFF
	11	11	0xB000_0000_0000	0xBFFF_FFFF_FFFF
3	12	12	0xC000_0000_0000	0xCFFF_FFFF_FFFF
	13	13	0xD000_0000_0000	0xDFFF_FFFF_FFFF
	14	14	0xE000_0000_0000	0xEFFF_FFFF_FFFF
	15	15	0xF000_0000_0000	0xFFFF_FFFF_FFFF

%* f!\$! %ZY\$\$(\$!\$ bcXYaUg_



5000L

\$I'

\$I + \$I Z

3.2

' 7) \$\$\$@ (%* 88F <H

\$I \$ \$I %\$\$\$\$\$\$\$\$\$\$\$\$ ((

((



3C5000L

0x2208	CORE2_WIN1_BASE	0x2308	CORE3_WIN1_BASE
0x2210	CORE2_WIN2_BASE	0x2310	CORE3_WIN2_BASE
0x2218	CORE2_WIN3_BASE	0x2318	CORE3_WIN3_BASE

3C5000L

0x2478	SCACHE0_WIN7_MASK	0x2578	SCACHE1_WIN7_MASK
0x2480	SCACHE0_WIN0_MMAP	0x2580	SCACHE1_WIN0_MMAP
0x2488	SCACHE0_WIN1_MMAP	0x2588	SCACHE1_WIN1_MMAP
0x2490	SCACHE0_WIN2_MMAP	0x2590	SCACHE1_WIN2_MMAP
0x2498	SCACHE0_WIN3_MMAP	0x2598	SCACHE1_WIN3_MMAP
0x24a0	SCACHE0_WIN4_MMAP	0x25a0	SCACHE1_WIN4_MMAP
0x24a8	SCACHE0_WIN5_MMAP	0x25a8	SCACHE1_WIN5_MMAP
0x24b0	SCACHE0_WIN6_MMAP	0x25b0	SCACHE1_WIN6_MMAP
0x24b8	SCACHE0_WIN7_MMAP	0x25b8	SCACHE1_WIN7_MMAP
0x2600	SCACHE2_WIN0_BASE	0x2700	SCACHE3_WIN0_BASE
0x2608	SCACHE2_WIN1_BASE	0x2708	SCACHE3_WIN1_BASE
0x2610	SCACHE2_WIN2_BASE	0x2710	SCACHE3_WIN2_BASE
0x2618	SCACHE2_WIN3_BASE	0x2718	SCACHE3_WIN3_BASE
0x2620	SCACHE2_WIN4_BASE	0x2720	SCACHE3_WIN4_BASE
0x2628	SCACHE2_WIN5_BASE	0x2728	SCACHE3_WIN5_BASE
0x2630	SCACHE2_WIN6_BASE	0x2730	SCACHE3_WIN6_BASE
0x2638	SCACHE2_WIN7_BASE	0x2738	SCACHE3_WIN7_BASE
0x2640	SCACHE2_WIN0_MASK	0x2740	SCACHE3_WIN0_MASK
0x2648	SCACHE2_WIN1_MASK	0x2748	SCACHE3_WIN1_MASK
0x2650	SCACHE2_WIN2_MASK	0x2750	SCACHE3_WIN2_MASK
0x2658	SCACHE2_WIN3_MASK	0x2758	SCACHE3_WIN3_MASK
0x2660	SCACHE2_WIN4_MASK	0x2760	SCACHE3_WIN4_MASK
0x2668	SCACHE2_WIN5_MASK	0x2768	SCACHE3_WIN5_MASK
0x2670	SCACHE2_WIN6_MASK	0x2770	SCACHE3_WIN6_MASK
0x2678	SCACHE2_WIN7_MASK	0x2778	SCACHE3_WIN7_MASK
0x2680	SCACHE2_WIN0_MMAP	0x2780	SCACHE3_WIN0_MMAP
0x2688	SCACHE2_WIN1_MMAP	0x2788	SCACHE3_WIN1_MMAP
0x2690	SCACHE2_WIN2_MMAP	0x2790	SCACHE3_WIN2_MMAP
0x2698	SCACHE2_WIN3_MMAP	0x2798	SCACHE3_WIN3_MMAP
0x26a0	SCACHE2_WIN4_MMAP	0x27a0	SCACHE3_WIN4_MMAP
0x26a8	SCACHE2_WIN5_MMAP	0x27a8	SCACHE3_WIN5_MMAP
0x26b0	SCACHE2_WIN6_MMAP	0x27b0	SCACHE3_WIN6_MMAP
0x26b8	SCACHE2_WIN7_MMAP	0x27b8	SCACHE3_WIN7_MMAP
-	-	0x2900	IO_L2X_WIN0_BASE
-	-	0x2908	IO_L2X_WIN1_BASE
-	-	0x2910	IO_L2X_WIN2_BASE
-	-	0x2918	IO_L2X_WIN3_BASE

3C5000L

-	-	0x2920	IO_L2X_WIN4_BASE
-	-	0x2928	IO_L2X_WIN5_BASE
-	-	0x2930	IO_L2X_WIN6_BASE
-	-	0x2938	IO_L2X_WIN7_BASE
-	-	0x2940	IO_L2X_WIN0_MASK
-	-	0x2948	IO_L2X_WIN1_MASK
-	-	0x2950	IO_L2X_WIN2_MASK
-	-	0x2958	IO_L2X_WIN3_MASK
-	-	0x2960	IO_L2X_WIN4_MASK
-	-	0x2968	IO_L2X_WIN5_MASK
-	-	0x2970	IO_L2X_WIN6_MASK
-	-	0x2978	IO_L2X_WIN7_MASK
-	-	0x2980	IO_L2X_WIN0_MMAP
-	-	0x2988	IO_L2X_WIN1_MMAP
-	-	0x2990	IO_L2X_WIN2_MMAP
-	-	0x2998	IO_L2X_WIN3_MMAP
-	-	0x29a0	IO_L2X_WIN4_MMAP
-	-	0x29a8	IO_L2X_WIN5_MMAP
-	-	0x29b0	IO_L2X_WIN6_MMAP
-	-	0x29b8	IO_L2X_WIN7_MMAP
0x2a00	HT0_LO_WIN0_BASE	0x2b00	HT0_HI_WIN0_BASE
0x2a08	HT0_LO_WIN1_BASE	0x2b08	HT0_HI_WIN1_BASE
0x2a10	HT0_LO_WIN2_BASE	0x2b10	HT0_HI_WIN2_BASE
0x2a18	HT0_LO_WIN3_BASE	0x2b18	HT0_HI_WIN3_BASE
0x2a20	HT0_LO_WIN4_BASE	0x2b20	HT0_HI_WIN4_BASE
0x2a28	HT0_LO_WIN5_BASE	0x2b28	HT0_HI_WIN5_BASE
0x2a30	HT0_LO_WIN6_BASE	0x2b30	HT0_HI_WIN6_BASE
0x2a38	HT0_LO_WIN7_BASE	0x2b38	HT0_HI_WIN7_BASE
0x2a40	HT0_LO_WIN0_MASK	0x2b40	HT0_HI_WIN0_MASK
0x2a48	HT0_LO_WIN1_MASK	0x2b48	HT0_HI_WIN1_MASK
0x2a50	HT0_LO_WIN2_MASK	0x2b50	HT0_HI_WIN2_MASK
0x2a58	HT0_LO_WIN3_MASK	0x2b58	HT0_HI_WIN3_MASK
0x2a60	HT0_LO_WIN4_MASK	0x2b60	HT0_HI_WIN4_MASK
0x2a68	HT0_LO_WIN5_MASK	0x2b68	HT0_HI_WIN5_MASK
0x2a70	HT0_LO_WIN6_MASK	0x2b70	HT0_HI_WIN6_MASK
0x2a78	HT0_LO_WIN7_MASK	0x2b78	HT0_HI_WIN7_MASK
0x2a80	HT0_LO_WIN0_MMAP	0x2b80	HT0_HI_WIN0_MMAP
0x2a88	HT0_LO_WIN1_MMAP	0x2b88	HT0_HI_WIN1_MMAP



3C5000L

3C5000L

0x2e38	HT1_LO_WIN7_BASE	0x2f38	HT1_HI_WIN7_BASE
0x2e40	HT1_LO_WIN0_MASK	0x2f40	HT1_HI_WIN0_MASK
0x2e48	HT1_LO_WIN1_MASK	0x2f48	HT1_HI_WIN1_MASK
0x2e50	HT1_LO_WIN2_MASK	0x2f50	HT1_HI_WIN2_MASK
0x2e58	HT1_LO_WIN3_MASK	0x2f58	HT1_HI_WIN3_MASK
0x2e60	HT1_LO_WIN4_MASK	0x2f60	HT1_HI_WIN4_MASK
0x2e68	HT1_LO_WIN5_MASK	0x2f68	HT1_HI_WIN5_MASK
0x2e70	HT1_LO_WIN6_MASK	0x2f70	HT1_HI_WIN6_MASK
0x2e78	HT1_LO_WIN7_MASK	0x2f78	HT1_HI_WIN7_MASK
0x2e80	HT1_LO_WIN0_MMAP	0x2f80	HT1_HI_WIN0_MMAP
0x2e88	HT1_LO_WIN1_MMAP	0x2f88	HT1_HI_WIN1_MMAP
0x2e90	HT1_LO_WIN2_MMAP	0x2f90	HT1_HI_WIN2_MMAP
0x2e98	HT1_LO_WIN3_MMAP	0x2f98	HT1_HI_WIN3_MMAP
0x2ea0	HT1_LO_WIN4_MMAP	0x2fa0	HT1_HI_WIN4_MMAP
0x2ea8	HT1_LO_WIN5_MMAP	0x2fa8	HT1_HI_WIN5_MMAP
0x2eb0	HT1_LO_WIN6_MMAP	0x2fb0	HT1_HI_WIN6_MMAP
0x2eb8	HT1_LO_WIN7_MMAP	0x2fb8	HT1_HI_WIN7_MMAP

I VUf & =C! F=B; (G\W\X\Y (\$! &(11) * + =C! F=B; - () * + - 65G9 A5G? AA5D *(65G9 ? A5G? % AA5D

3- 7MMAP

[63:48]	[47 10]	[7 4]	[3 0]

3- 8

0-3	Scache0-3
4-5	MC0-1
a	HT0_lo
b	HT0_hi
c	SE
d	MISC



3C5000L

e	HT1_lo
f	HT1_hi

4

' 7) \$\$\$@

' 7) \$\$\$@ (

\$! %ZY\$\$\$\$\$

=C7GF

7GF05006Q

5 =C7GF

6

6

4.1

0x0000

\$! %ZY\$\$\$\$\$

\$! \$\$\$

4- 1

7:0	Version	R	8'h11	
-----	---------	---	-------	--

4.2

0x0008

\$! \$\$\$,

4- 2

0	Centigrade	R	1'b1	1	CSR[0x428]
1	Node counter	R	1'b1	1	CSR[0x408]
2	MSI	R	1'b1	1	MSI
3	EXT_IOI	R	1'b1	1	EXT_IOI
4	IPL_percore	R	1'b1	1	CSR IPI
5	Freq_percore	R	1'b1	1	CSR
6	Freq_scale	R	1'b1	1	
7	DVFS_v1	R	1'b1	1	v1
8	Tsensor	R	1'b1	1	



13 MC1_clken

RW 1'b1 _

57:56	Bad_ip_ddr	R		2	DDR
61:60	Bad_ip_ht	R		2	HT

4.8

0x0198

\$! \$%,

4- 8

15:0		R		
19:16		R		
20	dotest	R		Dotest
21	iccc_en	R		Iccc_en
23:22		R		
24	Thsens0_overflow	R		0
25	Thsens1_overflow	R		1



#8=JSF9: 7 † 8=JS@CCD7 # 8=JSCI H

%%\$A<n &) A<n

3C5000L

[34:32]	VDDA_LDO_CTRL	RW		
[35]	VDDA_LDO_BYPASS	RW		
[38:36]	VDDD_LDO_CTRL	RW		
[39]	VDDD_LDO_BYPASS	RW		
[40]	VDDA_LDO_EN	RW		
[41]	VDDD_LDO_EN	RW		
		RW		

4.10

0x01D0

%%\$bg

\$! \$%\$

4- 11

2:0	core0_freqctrl	RW	0x7	0
3	core0_en	RW	0x1	0
6:4	core1_freqctrl	RW	0x7	1
7	core1_en	RW	0x1	1
10:8	core2_freqctrl	RW	0x7	2
11	core2_en	RW	0x1	2
14:12	core3_freqctrl	RW	0x7	3
15	core3_en	RW	0x1	3
			:	+1 /8

4.11

0x01D8

fYgYhb \$

fYgYhbSdfY \$)\$\$

fYgYhbSdfY % fYgYhb %

\$! \$%\$,

4- 12

0	Core0_resetrn_pre	RW	0x1	0
1	Core0_resetrn	RW	0x1	0
2	Core1_resetrn_pre	RW	0x1	1

3C5000L

3	Core1_resetrn	RW	0x1	1'7(G) xf
4	Core2_resetrn_pre	RW	0x1	2
5	Core2_resetrn	RW	0x1	2
6	Core3_resetrn_pre	RW	0x1	3
7	Core3_resetrn	RW	0x1	3

4.12

0x0400

\$! \$(\$\$

4- 13



3:0	scid_sel	RW	0x1E
7:4	Node_mask	RW	0xF
8	xrouter_en		

0x

24
ZPE61

46:44	freqscale_stable	RW	OxO	Stable clock
47	clken_stable	RW	OxO	Stable clock
48	EXT_INT_en	RW	OxO	IO
49	INT_encode	RW	OxO	
53:52				
54				
57:56	thsensor_sel	RW	OxO	
62:60	Auto_scale	R	OxO	
63	Auto_scale_doing	R	OxO	

4.14 Ox0428

\$I \$(&

7GF0\$! \$\$\$, 00\$Q

4- 15

7:0	Centigrade temperature	RO	OxO	
63:8		RW	OxO	

4.15 SRAM Ox0430

GfUa

\$I \$(' '\$

4- 16 SRAM

31:0	sram_ctrl	RW	OxO	Sram
63:32		RW	OxO	

4.16 FUSE0 Ox0460

: i gY\$

\$I \$(' *\$

4- 17 FUSE

127:0	Fuse_0	RW	OxO	
-------	--------	----	-----	--



4.17 FUSE1

0x0470

: i gY%

\$! \$(+\$

4- 18 FUSE

127:0	Fuse_1	RW	OxO	



5

' 7) \$\$\$

3C5000L

IA132 Clock	Main Clock	* 1			IA132 1GHz
Stable Clock	SYS_CLOCK	* 1			
Mem Clock	MEM PLL	PLL			
	Main Clock	/2 /4 /8			

5.2

				Q: (n+1)/8 I: 1/(n+1)
--	--	--	--	--------------------------

5.2.2

' 7) \$\$\$@

\$! %ZY\$\$\$\$\$

\$! \$(&\$

5- 4

22	freqscale_percore	RW	OxO	
23	clken_percore	RW	OxO	

ZfYegWU` YSdYfWtY

%

ZfYegWU` Y

ZfYegWU` YSacXY

W_YbSdYfWtY

%

W_Yb

\$! %\$) \$

5- 5

4	freqscale_mode	RW	OxO	Q: (n+1)/8 I: 1/(n+1)
3	clken	RW	OxO	
2:0	freqscale	RW	OxO	

5.3

W_Yb



5.3.1

\$! %ZY\$\$\$\$\$

\$! % \$

5- 6



42:40 Nod

26:24	HIO_freq_scale_ctrl	RW	3'b111	HT	0
27	HIO_clken	RW	1'b1		HIO
30:28	HT1_freq_scale_ctrl	RW	3'b111	HT	1
31	HT1_clken	RW	1'b1		HT1

<H
 Ž% #, %# Ž%
 \$! %ZY\$\$\$\$\$ ' \$! \$(&\$
 <H VčfY WcW_ BcXY WcW_ BcXY WcW_

5- 10

39:38	freqscale_mode_HT	RW	0x0	HT	0: (n+1)/8 1: 1/(n+1)
-------	-------------------	----	-----	----	--------------------------

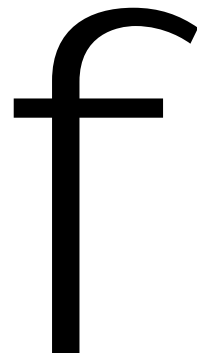
5.5 Stable Counter

GhUV Y 7ci bhYf

\$! %ZY\$\$\$\$\$ \$! \$(&\$

5- 11

20	stable_sel	RW	0x0	0 SYS CLOCK 1 NODE CLOCK
21	stable_reset	RW	0x0	1 0 Stable clock
40	freqscale_mode_stable	RW	0x0	0: (n+1)/8 1: 1/(n+1)
46:44	freqscale_stable	RW	0x0	Stable clock
47	clken_stable	RW	0x0	g: flž



6

' 7) \$\$\$@

Vłi bhYf #WładUfY

ghUV` Y Vłi bhYf

bcXY

Vłi bhYf

ghUV` Y Vłi bhYf

bcXY Vłi bhYf

6.1 Stable Counter

' 7) \$\$\$@

ghUV` Y Vłi bhYf

GhUV` Y Vłi bhYf

' 7) \$\$\$@

ghUV` Y Vłi bhYf

GhUV` Y Vłi hYf

6.1.1 Stable Timer

GhUV` Y Vłi bhYf

Vłi bhYf

h] aYf

GhUV` Y Vłi bhYf

GhUV` Y h] aYf

fX\kf 8F8H=A9

` cUX#ghcfY

7GF

6- 1

Core0_timer_config	0x1060	RW	0
Core0_timer_ticks	0x1070	R	0
Core1_timer_config	0x1160	RW	1
Core1_timer_ticks	0x1170	R	1
Core2_timer_config	0x1260	RW	2
Core2_timer_ticks	0x1270	R	2
Core3_timer_config	0x1360	RW	3
Core3_timer_ticks	0x1370	R	3

6- 2

percore_timer_config	0x1060	RW	
percore_timer_ticks	0x1070	R	

6- 3

timer_config				
63	1	RW	0x1	1 1
62	Periodic	RW	0x0	timer_config InitVal 1 0
61	Enable	RW	0x0	1
47:0	InitVal	RW	0x0	
timer_ticks				
63:48	0	R	0x0	0
47:0	Ticks	R	0x0	48'hffff_fff_fff

6.1.2 Stable Counter

GhUV` Y Vti bhYf

GhUV` Y Vti bhYf

\$! %ZY\$\$\$\$\$

\$! \$(&\$

6- 4

20	stable_sel	RW	0x0	0 SYS CLOCK 1 NODE CLOCK
21	stable_reset	RW	0x0	1 0
40	freqscale_mode_stable	RW	0x0	Stable clock 0: (n+1)/8 1: 1/(n+1)
46:44	freqscale_stable	RW	0x0	Stable clock
47	clken_stable	RW	0x0	Stable clock

7) \$\$\$@ É d +=GhU' Yci bhYb b c «a” ž

7D7:

e

l

D7: l% c

a”

D7: l

d

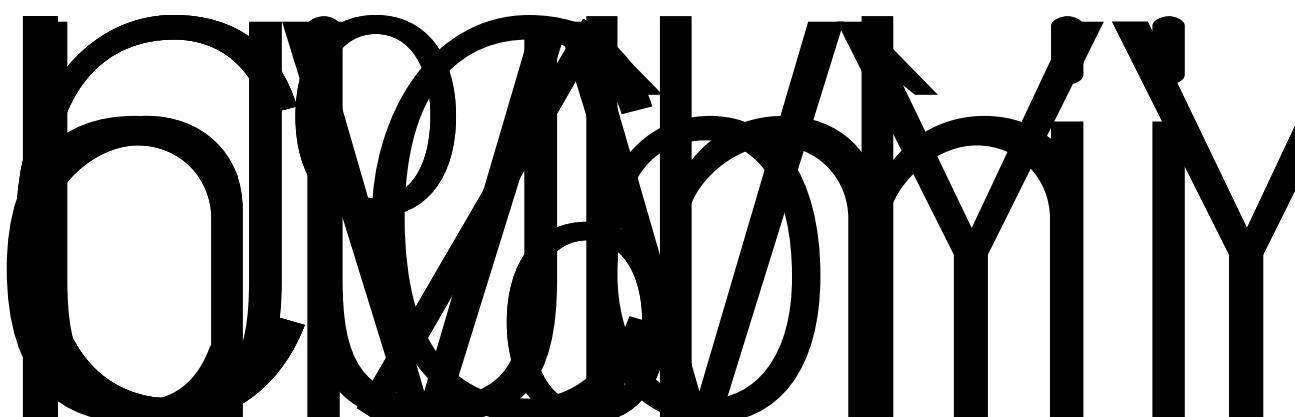
j^a

b 6=CG

c

7: e7: #7: ê d ž

GhUV` Yci bhYf b "%hUV`Y c izbhYf b bc



3C5000L

7 GPIO

' 7) \$\$\$@ ' & ; D=C
 ; D=C
 \$! %ZY\$\$\$\$\$

7.1 0x0500

\$! %ZY\$\$\$\$\$ \$! \$) \$\$

7- 1

7- 1				
31:0	GPIO_OEn	RW	32'hfffffff	GPIO
63:32	GPIO_FUNC_En	RW	32'hffff0000	GPIO

7.2 0x0508

\$! %ZY\$\$\$\$\$ \$! \$) \$,

7- 2

7- 2				
31:0	GPIO_O	RW	32'h0	GPIO
63:32	GPIO_I	RO	32'h0	GPIO

7.3 0x0510

\$! %ZY\$\$\$\$\$ \$! \$) %\$

7- 3

7- 3				
31:0	GPIO_INT_Pol	RW	32'h0	GPIO 0- 1-
63:32	GPIO_INT_en	RW	32'h0	GPIO

7.4 GPIO

' 7) \$\$\$@ ; D=C

; D=C\$\$; D=C%) ; D=C

=C

; D=C%* ; D=C % <H <H

=C <H\$#%\$<] #@cS<cghacXY

<H =C ; D=C

; D=C

7- 4 GPIO

; D=C			
\$; D=C\$\$	GD=S7Gb%	; D=C
%	; D=C\$%	GD=S7Gb&	; D=C
&	; D=C\$&	I 5FH%\$FL8	; D=C
'	; D=C\$'	I 5FH%\$HL8	; D=C
(; D=C\$(I 5FH%\$FHG	; D=C
)	; D=C\$)	I 5FH%\$7HG	; D=C
*	; D=C\$*	I 5FH%\$8HF	; D=C
+	; D=C\$+	I 5FH%\$8GF	; D=C
,	; D=C\$,	I 5FH%\$878	; D=C
-	; D=C\$-	I 5FH%\$F=	; D=C
\$\$; D=C%\$!	; D=C
%%	; D=C%%	!	; D=C
%&	; D=C%&	!	; D=C
%	; D=C%	G7BHSFGHb	; D=C
%{	; D=C%{	DFC7<CHb	; D=C
%)	; D=C%)	H<9FAHF=Db	; D=C
%*	<H\$S@CSDCK9FC?	; D=C%*	<H\$S@CSDCK9FC?
%+	<H\$S@CSFGHb	; D=C%+	<H\$S@CSFGHb
%	<H\$S@CS@8HSF9Eb	; D=C%	<H\$S@CS@8HSF9Eb
%	<H\$S@CS@8HSGHCDb	; D=C%	<H\$S@CS@8HSGHCDb

&\$	<H\$S<=SDCK9FC?	; D=C&\$	<H\$S<=SDCK9FC?
&%	<H\$S<=SFGHb	; D=C&%	<H\$S<=SFGHb
&&	<H\$S<=S@8HSF9Eb	; D=C&&	<H\$S<=S@8HSF9Eb
&'	<H\$S<=S@8HSGHCDb	; D=C&'	<H\$S<=S@8HSGHCDb
&(<H\$S@CS@SDCK9FC?	; D=C&(<H\$S@CS@SDCK9FC?
&)	<H\$S@CS@SFGHb	; D=C&)	<H\$S@CS@SFGHb
&*	<H\$S@CS@8HSF9Eb	; D=C&*	<H\$S@CS@8HSF9Eb
&+	<H\$S@CS@8HSGHCDb	; D=C&+	<H\$S@CS@8HSGHCDb
&	<H\$S<=SDCK9FC?	; D=C&	<H\$S<=SDCK9FC?
&-	<H\$S<=SFGHb	; D=C&-	<H\$S<=SFGHb
' \$	<H\$S<=S@8HSF9Eb	; D=C' \$	<H\$S<=S@8HSF9Eb
' %	<H\$S<=S@8HSGHCDb	; D=C' %	<H\$S<=S@8HSGHCDb

7.5 GPIO

' 7) \$\$\$@ ; D=C
; D=C\$\$; D=C\$, ; D=C%* ; D=C&(\$
; D=C\$% ; D=C\$- ; D=C%+ ; D=C&) %
; D=C\$& ; D=C%\$; D=C% ; D=C&* &
; D=C\$' ; D=C%& ; D=C% ; D=C&+ '
; D=C\$(; D=C%& ; D=C&\$; D=C&, (
; D=C\$) ; D=C% ; D=C&% ; D=C&-)
; D=C\$* ; D=C%(; D=C&& ; D=C' \$ *
; D=C\$+ ; D=C%& ; D=C&' ; D=C' % +

; D=C ; D=CS=BHSYb ; D=CS=BHSDC@

\$I %ZY\$\$\$\$\$ \$I \$) %\$

7- 5

31:0	GPIO_INT_Pol	RW	32'h0	GPIO 0-
------	--------------	----	-------	------------



3C5000L

				1 -
63:32	GPIO_INT_en	RW	32'h0	GPIO

; D=C

DC@ \$ %

8 LA 4 4

@5(*(*(

' 7) \$\$\$@

@5(*(7UVXY 5L= 7UVXY

@5(*(

CE @ccb[5fVX

CE

CE &)* , (

CE &)* *((,

CE

CE *(, &\$ (, &%& H@b *(H@b

CE 7UVXY 7UVXY *(?6 (

CE J]Vh]a 7UVXY 7UVXY

7

λ H B , D B 0
E J O ...)

W O A Q D e 8

K 8 1 2 4 E B D L

W O A Q D e 8

8 - E E @
E
J λ

W O A Q D e 8
W O A Q D e 8
W O A Q D e 8
W O A Q D e 8
W O A Q D e 8

H 2 1

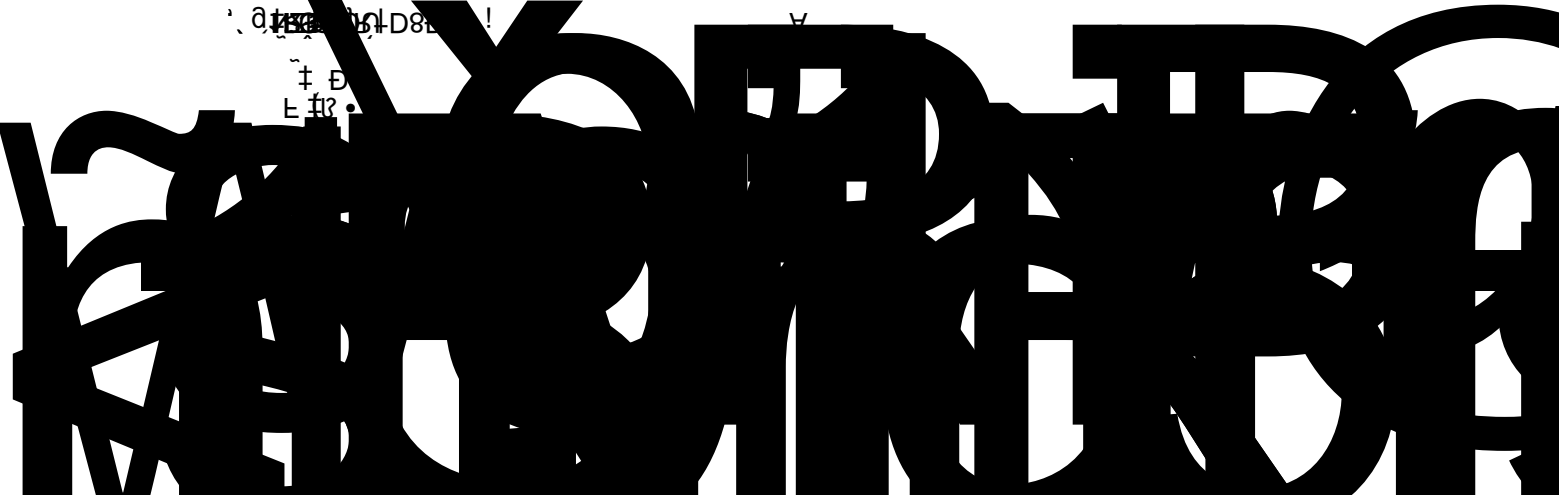
222@

x

λ H B , D B 0

λ H B , D B 0

λ H B , D B 0



\$

V] h55. 66

55 66 f155! 66Z%L

' 7) \$\$\$@

' 7) \$\$\$@

' 7) \$\$\$@

8- 1 ' 7) \$\$\$@



\$! \$	' % \$	DF=X				' & \%(SW\$%\$
	% \$	5F7<	&fV\$\$	@5' &	&fV\$%	& V%\$
			@5' &	&fV%\$	@5*(&fV%%
	&	D, AAI	%	AAI		% V%
	'	=C7GF	%	=C7GF		% V%
	%% (D5@9B			D5@9B	%
	%. %&	J5@9B			Ê	, X(+

\$! %

3C5000L

	%+. %	@@ HDSj Yf	%	' \%
	&%	@GDK	%	% V%
	&&	@5A	% 5A!	% V%
\$!	\$	778A5	% 7UWXY 7c\YfYbh 8A5	% V%
	%	G 6	% GhcfY :] ` ` 6i ZZYf G 6	% V%
	'	@@9L7	% @@	% V%
	(G78@M	% G7	% V%
)	@@865F	% @@ XVUf	% V%
	*	=H@6<A7	% =H@6 H@6	% V%
	+	=7<A7	% =7UWXY 87UWXY	% V%
	%,	GDKS@!	dU[Y kU' _	' \ (
	%%	GDKS<DS<:	% dU[Y kU' _ H@6	% V%
	%&	FJ5	%	% V%
	%*. %	FJA5L! %	% ! %	(\+
\$(' % \$	77S: F9E	<n	B#5
\$()	%\$. \$	77SAI @		B#5
	' % %*	77S8=J		B#5
\$! *	\$	DAD	%	% V%
	' . %	DAJ9F	%	' \%
	+. (DABI A	% ! %	(\'
	%, .	DA6=HG	% ! %	* \ ' Z
	%{	I DA	%	% V%
\$! U	\$	@% =! SDFYgYbh	% 7UWXY 7UWXY	% V%
	%	@% =! I b] Zm	% @% =! SDFYgYbh 7UWXY 7UWXY	% V\$
	&	@% 8 DfYgYbh	% 7UWXY	% V%
	'	@& =! DfYgYbh	% 7UWXY 7UWXY	% V%
	(@& =! I b] Zm	% @& =! SDFYgYbh 7UWXY 7UWXY	% V%
)	@& =! Df]j UhY	% @& =! SDFYgYbh 7UWXY	% V%
	*	@& =! =bWi gjj Y	% @& =! SDFYgYbh 7UWXY @%	% V\$
	+	@& 8 DfYgYbh	% 7UWXY	% V\$
	,	@& 8 Df]j UhY	% 7UWXY	% V\$

3C5000L

	-	@ 8 =bWi gj j Y	% 7UMXY @%	% V\$
	%\$	@ =l DfYgYbh	% 7UMXY 7UMXY	% V%
	%%	@ =l l b] Zm	% @ =l SdfYgYbh 7UMXY 7UMXY	% V%
	%&	@ =l Df]j UhY	% @ =l SdfYgYbh 7UMXY	% V\$
	%	@ =l =bWi gj j Y	% @ =l SdfYgYbh 7UMXY @% @&	% V%
	%{	@ 8 DfYgYbh	% 7UMXY	% V\$
	%}	@ 8 Df]j UhY	% 7UMXY	% V\$
	%*	@ 8 =bWi gj j Y	% 7UMXY @% @&	% V\$
\$! V	% . \$	KUn1 %	!% %\$ @ =l SdfYgYbh 7UMXY	%* \'
	& . %*	=bXYI ! `c[&	`c[&f1 7UMXY 7	, \,
	' \$. &(&	@] bYg] nY! `c[&	`c[&f17UMXY 7	, *
\$! W	% . \$	KUn1 %	!% %\$ @ 8 DfYgYbh 7UMXY	%* \'
	& . %*	=bXYI ! `c[&	`c[&f1 7UMXY 7	, \,
	' \$. &(&	@] bYg] nY! `c[&	`c[&f17UMXY 7	, *
\$! X	% . \$	KUn1 %	!% %\$ @ =l DfYgYbh 7UMXY	%* \Z
	& . %*	=bXYI ! `c[&	`c[&f1 7UMXY 7	, \,
	' \$. &(&	@] bYg] nY! `c[&	`c[&f17UMXY 7	, *
\$! Y	% . \$	KUn1 %	!% %\$ @ =l DfYgYbh 7UMXY	%* \Z
	& . %*	=bXYI ! `c[&	`c[&f1 7UMXY 7	, \,
	' \$. &(&	@] bYg] nY! `c[&	`c[&f17UMXY 7	, *

8.2 3C5000L

' 7) \$\$\$@ 7GF
7GF >H5;
7GF =C7GFF8" 6#<#K#8 =C7GFKF" 6#<#K#8
=C7GFF8" 6#<#K#8 =C7GFF8" 6#<#K#8 fXz f^ f^
7GF 7GF fX =C7GFKF" 6#<#K#8
=C7GFKF" 6#<#K#8 fXz f^ f^ 7GF
fX 7GF =C7GFF8" 6#<#K#8 =C7GFKF" 6#<#K#8

=C7GFF8" 6#<#K#8 =C7GFKF" 6#<#K#8
\$! %ZY\$\$\$\$\$



9 Cache SCache

G7UWY ' 7)

3C5000L

				3- 64-127 cycle random 4- 128-255 cycle random -
31	MCC storefill en	RW	1'b0	MCC storefill
34:32				
35	MCC clean exclusive replace en	RW	1'b0	
36	MCC clean shared replace en	RW	1'b0	



10

' 7) \$\$\$@ , =D= 6=CG

' 7) \$\$\$@ ' 5' \$\$\$

10.1

' 7) \$\$\$@ \$I ' ZZ\$\$\$\$\$\$ \$I %ZY\$\$\$\$\$\$
\$I ' ZZ\$\$\$\$\$\$ X] gUV` YS\$I ' ZZ\$
%\$- % %\$-)

10- 1



IPI_Status R 32 1
INT4 ä



3C5000L

Core0_IPI_Enalbe	0x1004	RW	0	IPI_Enalbe
Core0_IPI_Set	0x1008	W	0	IPI_Set
Core0_IPI_Clear	0x100c	W	0	IPI_Clear
Core0_MailBox0	0x10- - x0			

Core3_MailBox0	0x1320	R	3	IPI_MailBox0
Core3_MailBox1	0x1328	RW	3	IPI_MailBox1
Core3_MailBox2	0x1330	W	3	IPI_MailBox2
Core3_MailBox3	0x1338	W	3	IPI_MailBox3

' 7) \$\$\$@

' 7) \$\$\$@

77! BI A5

=D=

\$ \$

=D=SGhUhi g

\$! % 9\$%\$\$\$

%

\$

\$! %\$\$\$% 9\$%\$\$\$

10.2

' 7) \$\$\$@

10- 6

perCore_IPI_Status	0x1000	R	IPI_Status
perCore_IPI_Enalbe	0x1004	RW	IPI_Enalbe
perCore_IPI_Set	0x1008	W	IPI_Set
perCore_IPI_Clear	0x100c	W	IPI_Clear
perCore_MailBox0	0x1020	RW	IPI_MailBox0
perCore_MailBox1	0x1028	RW	IPI_MailBox1
perCore_MailBox2	0x1030	RW	IPI_MailBox2
perCore_MailBox3	0x1038	RW	IPI_MailBox3

AU] ` 6cl

10- 7

IPI_Send	0x1040	WO	32 [31] 1 [30:26] [25:16] [15:5] [4:0] IPI_Status
----------	--------	----	--



=D=SGYbX AU]` GYbX : fYe GYbX 5bm GYbX

10- 8

ANY_Send	0x1158	WO	64	
			[63:32]	
			[31]	1
			[30:27]	

11.1.1

' 5 \$\$\$ \$! %ZY\$\$\$\$\$
 \$! ' ZZ\$\$\$\$\$ \$! ' ZZ\$\$\$\$\$ X] gUV' YS\$! ' ZZ\$

11- 2 IO

Intisr	0x1420	32
Inten	0x1424	32
Intenset	0x1428	32
Intenclr	0x142c	32
Intedge	0x1434	32
CORE0_INTISR	0x1440	CORE0 32
CORE1_INTISR	0x1448	CORE1 32
CORE2_INTISR	0x1450	CORE2 32
CORE3_INTISR	0x1458	CORE3 32

' 7) \$\$\$@ (' & =BH\$ =BH
 7D\$SGhUhi g =D& =D) ' & =#C
 %% ' %% (\$! (' =BH&
 ' 7) \$\$\$@ 7GFO\$! (&\$QX - Q
 O+. (Q \$! + \$! + \$! & ' =BH&

11- 3

3:0	
7:4	

11- 4

Entry0	0x1400	GPIO24/16/8/0	Entry16	0x1410
--------	--------	---------------	---------	--------

Entry1	0x1401	GPIO25/17/9/1	Entry17	0x1411	HT0-int1
Entry2	0x1402	GPIO26/18/10/2	Entry18	0x1412	HT0-int2
Entry3	0x1403	GPIO27/19/11/3	Entry19	0x1413	HT0-int3
Entry4	0x1404	GPIO28/20/12/4	Entry20	0x1414	HT0-int4
Entry5	0x1405	GPIO29/21/13/5	Entry21	0x1415	HT0-int5
Entry6	0x1406	GPIO30/22/14/6	Entry22	0x1416	HT0-int6
Entry7	0x1407	GPIO31/23/15/7	Entry23	0x1417	HT0-int7
Entry8	0x1408	I2C0	Entry24	0x1418	HT1-int0
Entry9	0x1409	I2C1	Entry25	0x1419	HT1-int1
Entry10	0x140a	UART0	Entry26	0x141a	HT1-int2
Entry11	0x140b	MC0	Entry27	0x141b	HT1-int3
Entry12	0x140c	MC1	Entry28	0x141c	HT1-int4
Entry13	0x140d	SPI	Entry29	0x141d	HT1-int5
Entry14	0x140e	Thsens	Entry30	0x141e	HT1-int6
Entry15	0x140f	UART1	Entry31	0x141f	HT1-int7

11.1.2

' 7) \$\$\$@

11- 5

perCore_INTISR	0x1010	32
----------------	--------	----

11.2 I/O

&)* =C ' 7) \$\$\$@ =#C <H
<H =C

=C

\$! %ZY\$\$\$\$\$

\$! \$(&\$

11- 6

48	EXT_INT_en	RW	OxO	IO
----	------------	----	-----	----

=C

<H

&)*

11.2.1

=C

\$! %ZY\$\$\$\$\$

11- 7 IO

EXT_IOn[63:0]	0x1600	IO	[63:0]
EXT_IOn[127:64]	0x1608	IO	[127:64]
EXT_IOn[191:128]	0x1610	IO	[191:128]
EXT_IOn[255:192]	0x1618	IO	[255:192]

11- 8 IO

EXT_IObounce[63:0]	0x1680	IO	[63:0]
EXT_IObounce[127:64]	0x1688	IO	[127:64]
EXT_IObounce[191:128]	0x1690	IO	[191:128]
EXT_IObounce[255:192]	0x1698	IO	[255:192]

11- 9 IO

EXT_IOLsr[63:0]	0x1700	IO	[63:0]
EXT_IOLsr[127:64]	0x1708	IO	[127:64]
EXT_IOLsr[191:128]	0x1710	IO	[191:128]
EXT_IOLsr[255:192]	0x1718	IO	[255:192]



11- 10

IO



CORE0_EXT_IOLsr[63:0]	0x1800	0	IO	[63:0]
CORE0_EXT_IOLsr[127:64]	0x1808	0	IO	[127:64]
CORE0_EXT_IOLsr[191:128]	0x1810	0	IO	[191:128]
CORE0_EXT_IOLsr[255:192]				





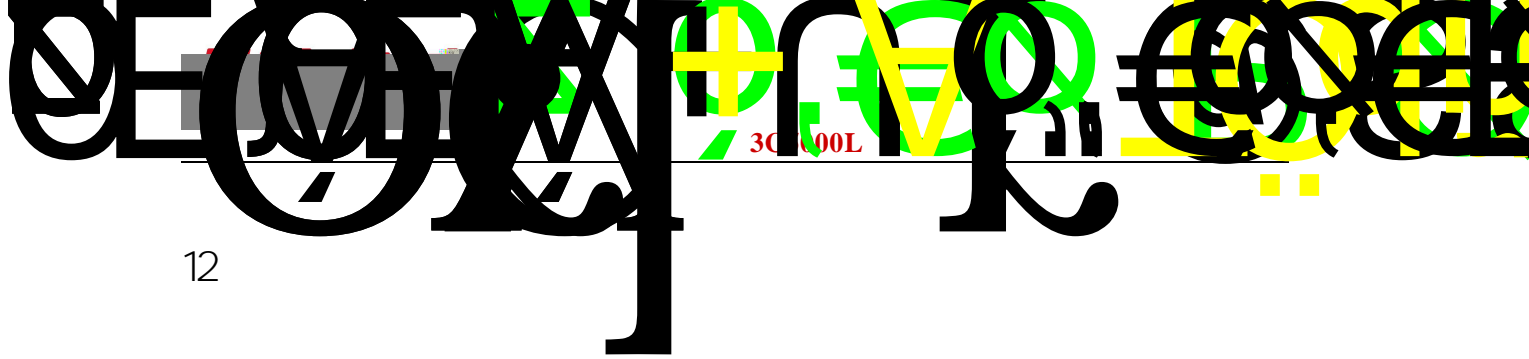


11.2.4

IO

HT

<H
 &)* (, <H
 <H=C
 (,
 =C <H <H
 &)* (, &)*
 =C <H
 <H <H \$I - \$\$\$\$YZXZV\$\$\$\$, \$
 <H
 =C =C \$I % \$\$



12

12.1

' 7) \$\$\$@

\$! % 9\$\$% ,

\$! % 9\$\$\$\$\$

\$! \$% ,

12- 1

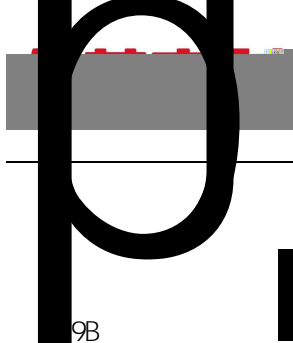


24

ThsensQ_overflow

R

0



; UhY

\$! %,

%*

9B

%

G9@

' 7) \$\$\$@

\$ %

(

\$! %ZY\$\$\$\$\$

12- 3



O+. \$Q <] S[UhY\$ \$

Q . . Q <] SYb\$ \$

O%% %\$Q <] SGY' \$ \$

O&' . %*Q <] S[UhY% %

O&(. &(Q <] SYb% %

O&+. &*Q <] SGY' % %

O - . ' &Q <] S[UhY& &

O(\$ (\$Q <] SYb& &

O(' . (&Q <] SGY' & &

O) . (, Q <] S[UhY' '

O)* .) *Q <] SYb' '

H\gYbgS] bhSWf` S<]

\$! %(*\$

FK

O) - .) , Q <] SGY' '

O+. \$Q @cS[UhY\$ \$

Q . . Q @cSYb\$ \$

O%% %\$Q @cSGY' \$ \$

O&' . %*Q @cS[UhY% %

O&(. &(Q @cSYb% %

O&+. &*Q @cSGY' % %

O - . ' &Q @cS[UhY& &

O(\$ (\$Q @cSYb& &

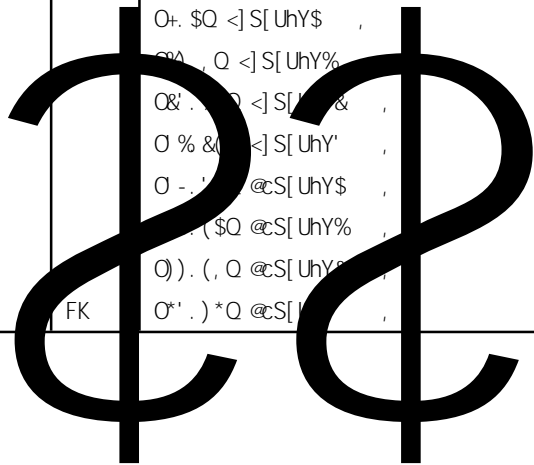
O(' . (&Q @cSGY' & &

H\gYbgS] bhSWf` S@c

\$! %(*,

FK

<p>HNgYbgS] bhSi d</p>	<p>\$l %(+,</p>	<p>FK O+. \$Q <] S[UhY\$, Q) , Q <] S[UhY% O& . Q <] S[UhY% O % & <] S[UhY' O - . ' @cS[UhY\$, (\$Q @cS[UhY% Q) . (, Q @cS[UhY% O* .) *Q @cS[</p>
------------------------	------------------	---



12.3

(

; 5H9

9B

%

G9@

' 7) \$\$\$@

: F9E

a"

<p>HNgYbgSZfYeSgWU' Y</p>	<p>\$l %(\$, \$</p>	<p>FK</p>	<p>O+. \$Q GWU' YS[UhY\$ \$ Q . . Q GWU' YSYb\$ \$ O% % \$Q GWU' YSGY' \$ \$ O% . %&Q GWU' YSZfYe\$ O& . %*Q GWU' YS[UhY% % O& . &(Q GWU' YSYb% % O&+ . &*Q GWU' YSGY' % % O \$. & Q GWU' YSZfYe% O - . ' &Q GWU' YS[UhY& & O(\$. (\$Q GWU' YSYb& & O(' . (&Q GWU' YSGY' & & O(* . ((Q GWU' YSZfYe& O) . (, Q GWU' YS[UhY' ' O) * .) *Q GWU' YSYb' ' O) - .) , Q GWU' YSGY' ' O* & * \$Q GWU' YSZfYe'</p>
<p>HNgYbgSZfYeSgWU' YSi d</p>	<p>\$l %(- \$</p>	<p>FK</p>	<p>O+. \$Q GWU' YS<] S[UhY\$, O% . , Q GWU' YS<] S[UhY% , O& . %*Q GWU' YS<] S[UhY& , O % &(Q GWU' YS<] S[UhY' , O - . ' &Q GWU' YS@S[UhY\$, O(+ . (\$Q GWU' YS@S[UhY% , O) . (, Q GWU' YS@S[UhY& , O* .) *Q GWU' YS@S[UhY' ,</p>

12.4

DFC7<CHb H<9FAHF=Db ; D=C%{
 ; D=C%{ DFC7<CHb H<9FAHF=Db
 DFC7<CHb
 DFC7<CHb \$
 df cW\chbSZfYeSgWU' Y DFC7<CHb
 df cW\chbScSgY' (
 H<9FAHF=Db h\Yf ahf] dbScSgY'
 (



3C5000L

11:9	Temp_cluster	RW	0	Thsens_trigger
------	--------------	----	---	----------------

=data*731/0x4000-273 -40 ~ 125

12- 7

Cluster

13 DDR4 SDRAM

' 7) \$\$\$@ 88F(G8F5A
>9G8+-!(

13.1 DDR4 SDRAM

' 7) \$\$\$@ 88D ' 8G 88D ,
7G , 88F(G8F5A (' 8G (7G ,
88F(G8F5A ' & F5B? && %
& 6Ub_ & 6Ub_ ; fci d F5Gb
75Gb KYb
' 7) \$\$\$@ 88F(

3C5000L

0x0028	rdfifo_empty(RD)				Overflow(RD)		
0x0030	dll_value(RD)	dll_init_done(RD)	dll_lock_mode	dll_bypass	dll_adj_cnt	dll_increment	dll_start_point
0x0038					dll_dbl_fix	dll_close_disable	dll_ck
0x0040					dbl_ctrl_ckca	dll_dbl_ckca	
0x0048	pll_ctrl_ckca			pll_lock_ckca(RD)	dll_lock_ckca(RD)	clken_ckca	clkssel_ckca
0x0050					dbl_ctrl_ds_0	dll_dbl_ds_0	
0x0058	pll_ctrl_ds_0			pll_lock_ds_0(RD)	dll_lock_ds_0(RD)	clken_ds_0	clkssel_ds_0
0x0060					dbl_ctrl_ds_1	dll_dbl_ds_1	
0x0068	pll_ctrl_ds_1			pll_lock_ds_1(RD)	dll_lock_ds_1(RD)	clken_ds_1	clkssel_ds_1
0x0070					dbl_ctrl_ds_2	dll_dbl_ds_2	
0x0078	pll_ctrl_ds_2			pll_lock_ds_2(RD)	dll_lock_ds_2(RD)	clken_ds_2	clkssel_ds_2
0x0080					dbl_ctrl_ds_3	dll_dbl_ds_3	
0x0088	pll_ctrl_ds_3			pll_lock_ds_3(RD)	dll_lock_ds_3(RD)	clken_ds_3	clkssel_ds_3
0x0090					dbl_ctrl_ds_4	dll_dbl_ds_4	
0x0098	pll_ctrl_ds_4			pll_lock_ds_4(RD)	dll_lock_ds_4(RD)	clken_ds_4	clkssel_ds_4
0x00a0					dbl_ctrl_ds_5	dll_dbl_ds_5	
0x00a8	pll_ctrl_ds_5			pll_lock_ds_5(RD)	dll_lock_ds_5(RD)	clken_ds_5	clkssel_ds_5
0x00b0					dbl_ctrl_ds_6	dll_dbl_ds_6	
0x00b8	pll_ctrl_ds_6			pll_lock_ds_6(RD)	dll_lock_ds_6(RD)	clken_ds_6	clkssel_ds_6
0x00c0					dbl_ctrl_ds_7	dll_dbl_ds_7	
0x00c8	pll_ctrl_ds_7			pll_lock_ds_7(RD)	dll_lock_ds_7(RD)	clken_ds_7	clkssel_ds_7
0x00d0					dbl_ctrl_ds_8	dll_dbl_ds_8	
0x00d8	pll_ctrl_ds_8			pll_lock_ds_8(RD)	dll_lock_ds_8(RD)	clken_ds_8	clkssel_ds_8
0x00e0	vrefclk_inv		vref_sample		vref_num	vref_dly	dll_vref
0x0100					dll_1xgen_0	dll_wrclk_0	dll_wrclk_0
0x0108					dll_rclk_1_0		
0x0110	rdodt_ctrl_0						

3C5000L

0x0168								rdqsn_bdy_0[35:32]
0x0170	rdq_bdy_0[24:21]	rdq_bdy_0[20:18]	rdq_bdy_0[17:15]	rdq_bdy_0[14:12]	rdq_bdy_0[11:9]	rdq_bdy_0[8:6]	rdq_bdy_0[5:3]	rdq_bdy_0[2:0]
0x0178								rdq_bdy_0[27:26]
0x0180					dll_1xcdly_1	dll_1xgen_1	dll_wrdqs_1	dll_wrdq_1
0x0188						dll_gate_1	dll_rddqs1_1	dll_rddqs0_1
0x0190	rdodt_ctrl_1	rdgate_len_1	rdgate_mode_1					



3C5000L

0x0288					dll_gate_3	dll_rddqs1_3	dll_rddqs0_3
0x0290	rdodt_ctrl_3	rdgate_len_3	rdgate_mode_3	rdgate_ctrl_3		dqs_oe_ctrl_3	dq_oe_ctrl_3
0x0298					dly_2x_3	redge_sel_3	rddqs_phase_3(RD)



3C5000L

0x03a8		w_bdy0_5[59:56]	w_bdy0_5[55:52]	w_bdy0_5[51:48]	w_bdy0_5[47:44]	w_bdy0_5[43:40]	w_bdy0_5[39:36]	w_bdy0_5[35:32]
0x03b0	w_bdy1_5[24:21]	w_bdy1_5[20:18]	w_bdy1_5[17:15]	w_bdy1_5[14:12]	w_bdy1_5[11:9]	w_bdy1_5[8:6]	w_bdy1_5[5:3]	w_bdy1_5[2:0]
0x03b8								w_bdy1_5[27:26]
0x03c0							rg_bdy_5[7:4]	rg_bdy_5[3:0]
0x03c8								
0x03d0	rdqsp_bdy_5[31:28]	rdqsp_bdy_5[27:24]	rdqsp_bdy_5[23:20]	rdqsp_bdy_5[19:16]	rdqsp_bdy_5[15:12]	rdqsp_bdy_5[11:8]	rdqsp_bdy_5[7:4]	rdqsp_bdy_5[3:0]
0x03d8								



3C5000L

0x04c8

0x04d0

rdqsp_bdlly_7f3




3C5000L

3C5000L

0x1300							ref_num	ref_sch_en
0x1308							Status_sref(RD)	srefresh_req
0x1340	hardware_pd_7	hardware_pd_6	hardware_pd_5	hardware_pd_4	hardware_pd_3	hardware_pd_2	hardware_pd_1	hardware_pd_0
0x1348	power_sta_7(RD)	power_sta_6(RD)	power_sta_5(RD)	power_sta_4(RD)	power_sta_3(RD)	power_sta_2(RD)	power_sta_1(RD)	power_sta_0(RD)
0x1350	selfref_age		slowpd_age		fastpd_age		active_age	
0x1358				power_up				Age_step
0x1360	tCONF_IDLE				tLPMC_IDLE			
0x1380								zq_overlap
0x1388								zq_stat_en
0x1390	zq_cnt_1(RD)				zq_cnt_0(RD)			
0x1398	zq_cnt_3(RD)				zq_cnt_2(RD)			
0x13a0	zq_cnt_5(RD)				zq_cnt_4(RD)			
0x13a8	zq_cnt_6(RD)				zq_cnt_6(RD)			
0x13c0					odt_wr_cs_map			
0x13c8							odt_wr_length	odt_wr_delay
0x13d0					odt_rd_cs_map			
0x13d8							odt_rd_length	odt_rd_delay
0x1400				tRESYNC_length	tRESYNC_delay	tRESYNC_shift	tRESYNC_max	tRESYNC_min
0x1440					pre_predict		tm_cmdq_num	burst_length
0x1448								ca_timing
0x1450						wr/rd_dbi_en	ca_par_en	crc_en
0x1458							tCA_PAR	tWR_CRC
0x1460	bit_map_7	bit_map_6	bit_map_5	bit_map_6	bit_map_3	bit_map_2	bit_map_1	bit_map_0
0x1468	bit_map_15	bit_map_14	bit_map_13	bit_map_12	bit_map_11	bit_map_10	bit_map_9	bit_map_8
0x1470							bit_map_17	bit_map_16
0x1478								bitmap_mirror
0x1480				alern_misc(RD)			alern_cnt	alern_clr
0x1488	alern_addr(RD)							
0x1500	win0_base							
0x1508	win1_base							
0x1510	win2_base							
0x1518	win3_base							
0x1520	win4_base							



3C5000L

0x2118	ba_conflict_all(RD)
0x2120	ba_conflict_last1(RD)
0x2128	ba_conflict_last2(RD)
0x2130	ba_conflict_last3(RD)
0x2138	ba_conflict_last4(RD)
0x2140	ba_conflict_last5(RD)
0x2148	ba_conflict_last6(RD)
0x2150	ba_conflict_last7(RD)
0x2158	ba_conflict_last8(RD)
0x2160	rd_conflict(RD)
0x2168	wr_conflict(RD)
0x2170	rtw_conflict(RD)
0x2178	

3C5000L

0x3038	lpbk_dat_w0[127:64]					
0x3040	lpbk_dat_w1[63:0]					
0x3048	lpbk_dat_w1[127:64]					
0x3050	lpbk_ecc_mask_w	lpbk_dat_mask_w0		lpbk_ecc_w0		
	0					
0x3058	lpbk_ecc_mask_w	lpbk_dat_mask_w1		lpbk_ecc_w1		
	1					
0x3060						prbs_23
0x3068				prbs_init		
0x3100				fix_data_pattern_index	bus_width	page_size
				x		test_engine_en
0x3108		cs_diff_tst	c_diff_tst	bg_diff_tst	ba_diff_tst	row_diff_tst
						col_diff_tst
0x3120	addr_base_tst					
0x3128						
0x3130	user_data_pattern					
0x3138						
0x3140	valid_bits[63:0]					
0x3148						
0x3150	ctrl[63:0]					
0x3158	ctrl[127:64]					
0x3160	obs[63:0] (RD)					
0x3168	obs[127:64] (RD)					
0x3170	obs[191:128] (RD)					
0x3178	obs[255:192] (RD)					
0x3180	obs[319:256] (RD)					
0x3188	obs[383:320] (RD)					
0x3190	obs[447:384] (RD)					
0x3198	obs[511:448] (RD)					
0x31a0	obs[575:512] (RD)					
0x31a8	obs[639:576] (RD)					
0x31b0	obs[671:640](RD)					
0x3200						
0x3208						



0x3308	tst_308
0x3310	tst_310
0x3318	tst_318
0x3320	tst_320
0x3328	tst_328
0x3330	tst_330
0x3338	tst_338
0x3340	tst_340
0x3348	tst_348
0x3350	tst_350
0x3358	tst_358
0x3360	tst_360
0x3368	tst_368
0x3370	tst_370
0x3378	tst_378

13.5

13.5.1

=b] hSghUf h \$l \$%\$ \$l & =b] hSghUf h

8F5A

f!%& daSW_SgY` SW_WU daSW_SgY` SXg
 fl&t daSd\n\$] b] hSghUf h % D<M
 fl t 8@@ daSX` ` S] b] hSXcbY %
 fl(t daSX` ` S` cW_Sl daSd` ` S` cW_Sl %
 fl) t daSW_YbSl
 fl* t daS] b] hSghUf h %
 fl+ t daSXf UaS] b] h daSWgSYbUV` Y

13.5.2

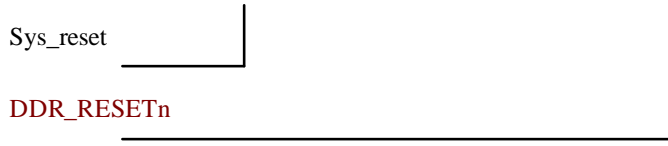
GHF dUXSfYgYhSdc \$l , \$,

88FSF9G9Hb



fYgYhSWf` 0% \$Q 11 & V\$\$
88FSF9G9Hb

,
,
,
,





; 5H9

8E

8E

V] h! XYg_Yk

XUhUg`]W

V] h

13.5.3.1 Write Leveling

Kf] hY @] Y`] b[8EG

f] %

f] & 8` Skf XegSI | 1 \$, \$! &\$

f] 8` Skf XeSI | 1 \$, \$! \$

f] (@` SacXY & V\$%

f]) @` SfYUXm % Kf] hY @] Y`] b[

f] * @` SfYe %

f] + @` SXcbY % Kf] hY @] Y`] b[

f] , @` SfYgdSI \$ 8` Skf XeSI O*. \$Q

 X` S% X` nO*. \$Q %)! + @` SfYgdSI % -

 % 8` Skf XeSI O*. \$Q X` S% X` nO*. \$Q %)! +

 @` SfYgdSI \$ 8` Skf XeSI O*. \$Q X` S% X` nO*. \$Q

 %)! + @` SfYgdSI % -

f] - 8` Skf XeSI X` S% X` m \$! (\$ 8` Skf XeSI X` S% X` m

f] %\$ 8=AA daSX` n&\$& \$! \$ daSX` n&\$&

 \$! %\$%\$%

f] %& @` SacXY \$! +\$\$ & V\$\$ Kf] hY @] Y`] b[

13.5.3.2 Gate Leveling

; UhY @] Y`] b[8EG

f] %

f] & Kf] hY @] Y`] b[

f] 8` S[UhYSI | 1 \$, \$

f] (@` SacXY & V\$%

f]) @` SfYUXm % ; UhY @] Y`] b[

f] * @` SfYe %

f] + @` SXcbY % ; UhY @] Y`] b[

f] , @` SfYgdSI O\$Q @` SfYgdSI O\$Q %

 8` S[UhYSI O*. \$Q % *! , \$



3C5000L

fl-Ł \$ 8`S[UhYSI O*. \$Q % *! -
 % ; UhY @/j Y`] b[
 fP%Ł daSfXXegSd\UgY daSfXYX[YSgY`
 fP%Ł 8`S[UhYSI I 1 \$, \$I &\$
 fP%Ł @`SfYe @`SfYgdSI O+.)Q
 @`SfYgdSI O(. &Q 6i fghS`Yb[h\#& %
 (FXScYSVY[] bSI
 6i fghS`Yb[h\#& 8`S[UhYSI
 fP%Ł @`SacXY \$I +\$\$ & V\$\$; UhY @/j Y`] b[
 fP%Ł ; UhY @/j Y`] b[

13.5.4

daSdLUXSWhf`SWJOSQ %
 daSdLUXSWhf`SWJOSQ \$ 88F(75@ AcXY

13.5.5 MRS mi

f(Ł	AfgSfYe	\$l %&*	%	8F5A	AFG
f)Ł	AfgSXcbY	\$l %&+		%	AFG
		\$			
f*Ł	7caaUbXSacXY	\$l %&\$		\$	

13.5.6

				8F5A		7aXSVg
7aXSWaX	7aXSVU	7aXSU	\$l %&		8F5A	

f)Ł	7aXSVg	7aXSWaX	7aXSVU	7aXSU	\$l %&
f)Ł	7caaUbXSacXY	\$l %&\$		%	
f' Ł	GhUhi gSWaX	\$l %&&		%	
		\$			
f(Ł	7aXsfYe	\$l %&%	%	8F5A	
f)Ł	7caaUbXSacXY	\$l %&\$		\$	

13.5.7

		hYghSd\m		hYghSd\m
hYghSl				hYghSd\m
daSl				

f)Ł			
f)Ł			
f' Ł	@V_SYb	%	
f(Ł	@V_SghUfh	%	

f) £

f*£ @dV_SYffcf %
@dV_Sf
\$

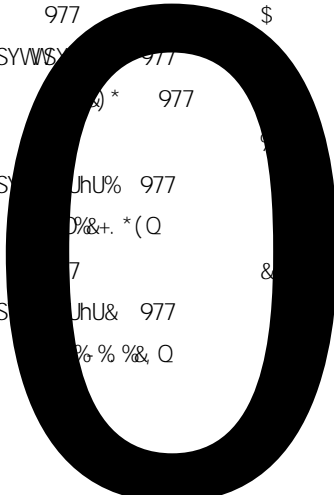
13.5.8 ECC

977 *(
9W\$YbUV Y \$! %& \$ &
9W\$YbUV YO\$Q 977 977
9W\$YbUV YO%Q 977
977 =bhSYbUV Y
=bhSj YW\$cf O\$Q 977 % &
=bhSj YW\$hf O%Q 977 =bhSj YW\$hf %

13.5.9

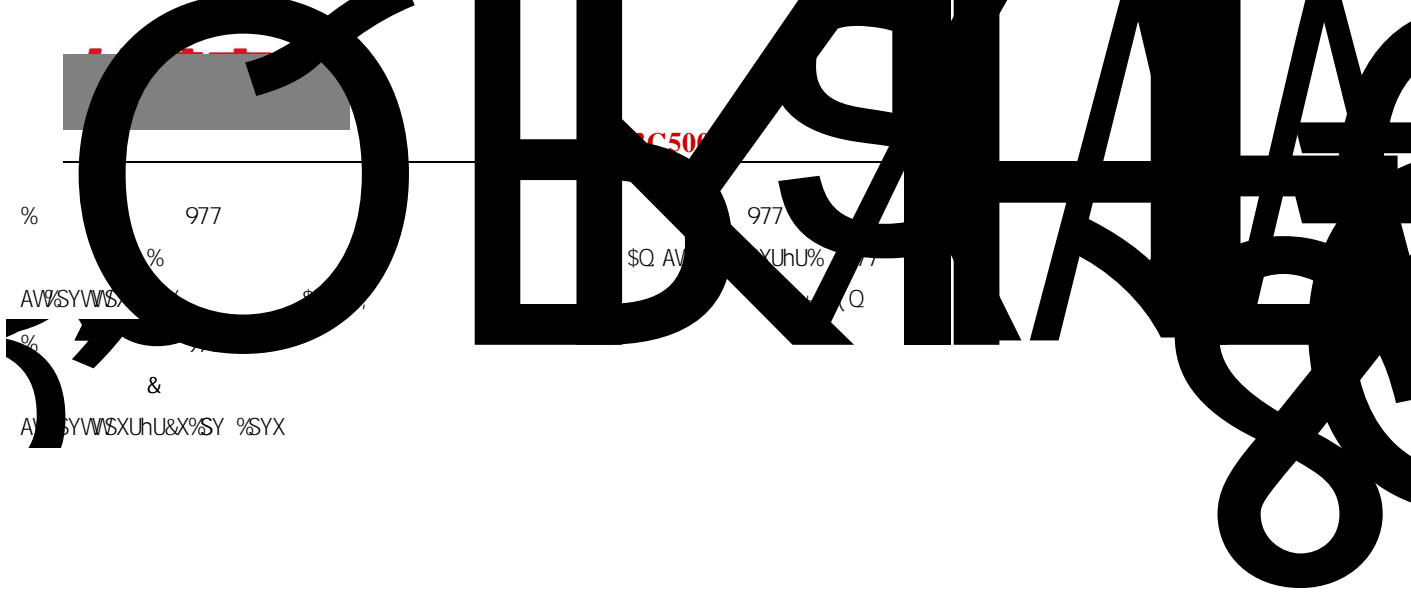


			\$	977		
			O+. \$Q	A7\$]bhSVh	977	
			O% , Q	A7\$]bhSVhSYffFfCk	977	
\$	977					
AV\$SYW\$Vh	\$! \$*%\$	FK	O& . %Q	A7\$]bhSVhSZUhU rIFCk	977	
			d\			
			\$	977		
			O+. \$Q	A7\$ YW\$VhSVgS\$ 7G\$	977	
			O% , Q	A7\$ YW\$VhSVgS% 7G%	977	
			O& . %Q	A7\$ YW\$VhSVgS& 7G&	977	
			O % &(Q	A7\$ YW\$VhSVgS' 7G	977	
			O - . ' &Q	A7\$ YW\$VhSVgS(7G(977	
\$	977		O+ . (\$Q	A7\$ YW\$VhSVgS) 7G)	977	
AV\$SYW\$VgSVh	\$! \$*%	FC	O) . (, Q	A7\$ YW\$VhSVgS* 7G*	977	
			O* .) *Q	A7\$ YW\$VhSVgS+ 7G+	977	
			\$	977		
			O+. \$Q	A7\$ YW\$VhXYS*(*(977	977
			O(% ' &Q	A7\$ YW\$VhXYS&)* &)*	977	977
			O) & (, Q	A7\$ YW\$VhXYSX] f	977	
\$	977					
AV\$SYW\$VtXY	\$! \$*&\$	FC	O* \$.) *Q	A7\$ YW\$XhUSX] f	977	
\$	977					
AV\$SYW\$SUXf	\$! \$*&	FC	\$	977		
\$	977		O* . \$Q	A7\$ YW\$SUXf	977	
\$			O* . \$Q	AV\$SYW\$S	977	*(
AV\$SYW\$XhUS	\$! \$* \$	FC	977)*	977	O* . \$Q
\$	977		\$			
%			O* . \$Q	AV\$SYW\$XhU%	977	&)*
AV\$SYW\$XhU%	\$! \$* ,	FC	977	D%+ . *(Q		
\$	977		\$	7		&
&			O* . \$Q	AV\$SYW\$XhU&	977	&)*
AV\$SYW\$XhU&	\$! \$*(\$	FC	977	% % & Q		
\$	977					
AV\$SYW\$XhU	\$! \$*(,	A\$				



977

% 977 AW\$SYW\$gYh	\$! \$+\$\$	FK	% 977 O). \$Q A7%] bhSYbUV Y Q Q A7%] bhShf][[Yf O&% %Q A7%] bhSj YWfc fFfCŁ O ' . ' &Q A7% YW\$YbUV Y 977 O(\$Q A7% fXSVYZcfYSkf
	\$! \$+,\$	FK	
% 977 AW\$SYW\$Vbh	\$! \$+\$\$	FK	% 977 O+. \$Q A7%] bhSVbh 977 O% . , Q A7%] bhSVbhSYffFfCŁ 977 O& . %Q A7%] bhSVbhSZUhU fFfCŁ 977
% 977 AW\$SYW\$VgSVbh	\$! \$+%	FC	% 977 O+. \$Q A7% YW\$SVbhSVgS\$ 7G\$ 977 O% . , Q A7% YW\$SVbhSVgS% 7G% 977 O& . %Q A7% YW\$SVbhSVgS& 7G& 977 O % &(Q A7% YW\$SVbhSVgS' 7G' 977 O - . ' &Q A7% YW\$SVbhSVgS(7G(977 O(+. (\$Q A7% YW\$SVbhSVgS) 7G) 977 O) . (, Q A7% YW\$SVbhSVgS* 7G* 977 O* .) *Q A7% YW\$SVbhSVgS+ 7G+ 977
% 977 AW\$SYW\$VtXY	\$! \$+&\$	FC	% 977 O+. \$Q A7% YW\$SVtXY\$*(*(977 977 O(\$ ' &Q A7% YW\$SVtXY\$)* &)* 977 977 O) & (, Q A7% YW\$SVtXY\$X] f 977 O* \$.) *Q A7% YW\$SXUhUSX] f 977
% 977 AW\$SYW\$SUXxf	\$! \$+&	FC	% 977 O* . \$Q A7% YW\$SUXxf 977
% 977 AW\$SYW\$XUhUS	\$! \$+' \$	FC	% 977 \$ O* . \$Q AW\$SYW\$XUhUS 977 *(977 &)* 977 O* . \$Q



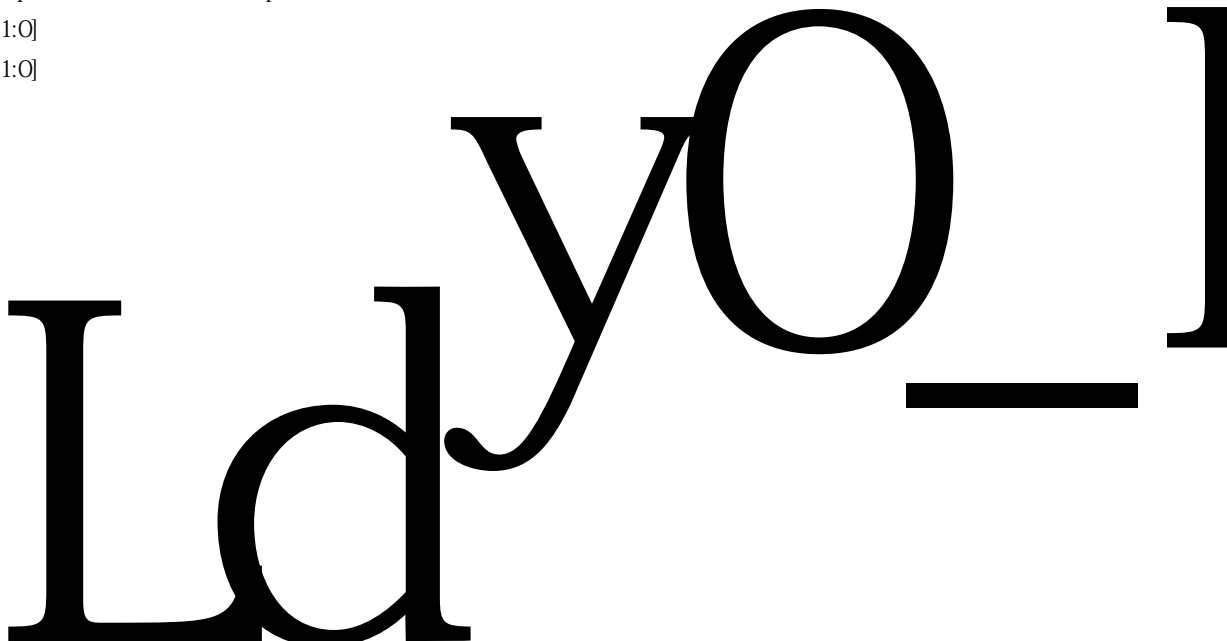


14 HyperTransport

' 7) \$\$\$@



HIO_8x2	1	16	HyperTransport	8
			HIO_Lo address[40] = 0	
			HIO_Hi address[40] = 1;	
			1	
HIO_Lo_mode	1	HIO_Lo		
		HIO_Lo		HIO_Lo_Powerok
		HIO_Lo_Rstn	HIO_Lo_Ldt_Stopn	
				"Act
		as Slave"	0	HyperTransport
		Bridge	1	0
		0	HyperTransport	
			P2P	
			1	
	0	HIO_Lo		
				HIO_Lo_Powerok
		HIO_Lo_Rstn	HIO_Lo_Ldt_Stopn	
				HT
HIO_Lo_Powerok	Powerok	HyperTransport	Powerok	
		HIO_Lo_Mode	1	HIO_Lo
		HIO_Lo_Mode	0	
HIO_Lo_Rstn	Rstn	HyperTransport	Rstn	
		HIO_Lo_Mode	1	HIO_Lo
		HIO_Lo_Mode	0	
HIO_Lo_Ldt_Stopn	Ldt_Stopn	HyperTransport	Ldt_Stopn	
		HIO_Lo_Mode	1	HIO_Lo
		HIO_Lo_Mode	0	
HIO_Lo_Ldt_Reqn	Ldt_Reqn	HyperTransport	Ldt_Reqn	
HIO_Hi_mode				
HIO_Hi_Powerok	Powerok			
HIO_Hi_Rstn	Rstn			
HIO_Hi_Ldt_Stopn	Ldt_Stopn			
HIO_Hi_Ldt_Reqn	Ldt_Reqn			
HIO_Rx_CLKp[1:0]				
HIO_Rx_CLKn[1:0]				



HTO_Rx_CADp[15:0]	CAD[15:0]	HyperTransport CAD
HTO_Rx_CADn[15:0]		[15:8]
HTO_Tx_CADp[15:0]		
HTO_Tx_CADn[15:0]		

<rdYf Hf Ubgdcf h <rdYf Hf Ubgdcf h

fI&\$\$A<nŁ fI, V] hŁ

=b] h 7cad` YhY %(")" &

@ b_ K] Xh\ Ć h @ b_ K] Xh\ =b %(")" &

@ b_ K] Xh\ Ć h @ b_ K] Xh\ =b @ b_

: fYe

<HS@XhSGhcdb

<rdYf Hf Ubgdcf h <rdYf Hf Ubgdcf h

<rdYf Hf Ubgdcf h

14.2 HyperTransport

' 7) \$\$\$@ <rdYf Hf Ubgdcf h % '\$' #' "\$

<rdYf Hf Ubgdcf h <rdYf Hf Ubgdcf h

14- 2 HyperTransport

000000	-	NOP		
000001	NPC	FLUSH		
x01xxx	NPC or PC	Write	bit 5 0 - Nonposted 1 - Posted bit 2 0 - Byte 1 - Doubleword bit 1 Don't Care bit 0 Don't Care	bit 5 1 POSTED bit 2 0 - Byte 1 - Doubleword bit 1 Don't Care bit 0 1
01xxxx	NPC	Read	bit 3 Don't Care bit 2 0 - Byte 1 - Doubleword bit 1 Don't Care bit 0 Don't Care	bit 3 Don't Care bit 2 0 - Byte 1 - Doubleword bit 1 Don't Care bit 0 1
110000	R	RdResponse		
110011	R	TgtDone		
110100	PC	WrCoherent	----	
110101	PC	WrAddr	----	

111000	R	RespCoherent	----	
111001	NPC	RdCoherent	----	
111010	PC	Broadcast		
111011	NPC	RdAddr	----	
111100	PC	FENCE		
111111	-	Sync/Error	Sync/Error	

14- 3

000000	-	NOP		
x01x0x	NPC or PC	Write	bit 5 0- Nonposted 1 - Posted bit 2 0- Byte 1 - Doubleword bit 0 0	bit 5 1 POSTED bit 2 0- Byte 1 - Doubleword bit 0 1
010x0x	NPC	Read	bit 2 0- Byte 1 - Doubleword bit 0 Don't Care	bit 2 0- Byte 1 - Doubleword bit 0 1
110000	R	RdResponse		
110011	R	TgtDone		
110100	PC	WrCoherent	----	
110101	PC	WrAddr	----	
111000	R	RespCoherent	----	
111001	NPC	RdCoherent	----	
111011	NPC	RdAddr	----	
111111	-	Sync/Error		

14.3 HyperTransport

<mdYfHfUbgdcfh &)* :|l 5fVjhYf

9C=

%(")" +

14.3.1 PIC

D=7

D=7

D=7

D=7

D=7

D=7

D=7

(

D=7

' 7) \$\$\$@ <mdYfHfUbgdcfh

D=7



&)*

(

D=7

14.3.2

<H

<H

<H

7DI

<H

<H

\$I - \$\$\$\$YI

14.4 HyperTransport

14.4.1 HyperTransport

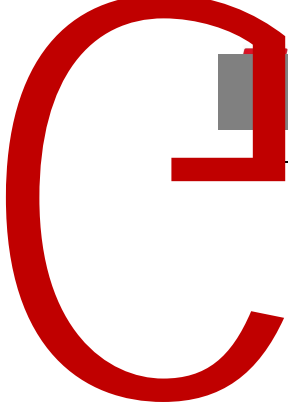
' 7) \$\$\$@

(<rdYfHfUbgdcfh

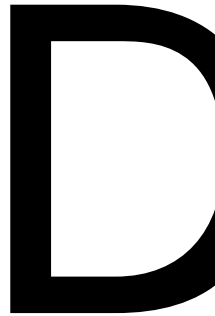
14- 5 4 HyperTransport

0x0A00_0000_0000	0x0AFF_FFFF_FFFF	1 Tbytes	HIO_LO
0x0B00_0000_0000	0x0BFF_FFFF_FFFF	1 Tbytes	HIO_HI
0x0E00_0000_0000	0x0EFF_FFFF_FFFF	1 Tbytes	HT1_LO
0x0F00_0000_0000	0x0FFF_FFFF_FFFF	1 Tbytes	HT1_HI

				act_as_slave	0	
14.5.10	3	HyperTransport	HyperTransport	P2P HyperTransport		
				act_as_slave	1	
Post 14.5.12	2		HyperTransport Post Write	Post Write HyperTransport		
14.5.13	2		Cache	HT HyperTransport		IO
				HyperTransport		
Uncache 14.5.14	2	HyperTransport	HyperTransport Uncache	DMA Cache		IO



3C5000L



\$! %\$
\$! %
\$! %
\$! %W
\$! &\$
\$! &
\$! &

7UfXVi g 7=G Dc] bhYf

3C5000L

	\$! - 7	=BH JYVhcf Q&). &&(Q		
	\$! 5\$	=BH 9bUV Y0 % \$Q		
	\$! 5(=BH 9bUV Y0* . ' &Q		
	\$! 5,	=BH 9bUV Y0-). *(Q		
	\$! 57	=BH 9bUV Y0%&+. - *Q		
	\$! 6\$	=BH 9bUV Y0% - . %& Q		
	\$! 6(=BH 9bUV Y0% % % \$Q		
	\$! 6,	=BH 9bUV Y0&& . % &Q		
	\$! 67	=BH 9bUV Y0&). &&(Q		
75D) ; Yb'	\$! 7\$	7UdUM] `] hm HrdY	7Ud 9bi a#=bXYI	7UdUM] `] hm Dc] bhYf
	\$! 7(; `cVU @ b_ HFU] b] b[
	\$! 7,	HFUbg] hhYf 7cbZ] [i fUh] cb \$		
	\$! 77	FYW] j Yf 7cbZ] [i fUh] cb \$		
	\$! 8\$	@ b_ HFU] b] b[\$		
	\$! 8(: fYei YbWn 9l hYbg] cb		
	\$! 8,	HFUbg] hhYf 7cbZ] [i fUh] cb %		
	\$! 87	FYW] j Yf 7cbZ] [i fUh] cb %		
	\$! 9\$	@ b_ HFU] b] b[%		
	\$! 9(6=GH 7cbhfc'		

9bUV Y	\$! %\$\$	8Yj] W' =8		JYbXcf =8	
	\$! %\$(GhUhi g		7caaUbX	
	\$! %\$,	7 Ugg 7cXY			FYj] g] cb =8
	\$! %\$W	6=GH	<YUXYf HrdY	@hYbWn H] aYf	
	\$! %\$				
	\$! %\$(
	\$! %%				
	\$! %\$W				
	\$! %\$\$				
	\$! %\$(
	\$! %&	7UfXVi g 7=G Dc] bhYf			
	\$! %\$W	Gi VgnghYa =8	Gi VgnghYa JYbXcf =8		
	\$! % \$	9l dUbg] cb FCA 9bUV Y 5XXfYgg			
	\$! % (FYgYfj YX		7UdUM] `] h] Yg Dc] bhYf	
	\$! % ,	FYgYfj YX			
	\$! % W	6f] X[Y 7cbhfc'	=bhYffi dh D] b	=bhYffi dh @bY	
	FYW] j Y	\$! %(\$	<H FL 9bUV Y \$		

KJ bXckg	\$I %4 (<H FL AUg_ \$
	\$I %4,	<H FL 9bUV Y %
	\$I %47	<H FL AUg_ %
	\$I %9 \$	<H FL 9bUV Y &
	\$I %9 (<H FL AUg_ &
	\$I %9,	<H FL 9bUV Y '
	\$I %97	<H FL AUg_ '
	\$I %*\$	<H FL 9bUV Y (
	\$I %*(<H FL AUg_ (
<YUXYf HFUbg	\$I %*,	<H FL <YUXYf HFUbg
	\$I %*7	<H FL 9LH <YUXYf HFUbg
	\$I %+\$	<H HL Dcgh 9bUV Y \$
Dcgh	\$I %+(<H HL Dcgh AUg_ \$
KJ bXckg	\$I %+,	<H HL Dcgh 9bUV Y %
	\$I %+7	<H HL Dcgh AUg_ %
	\$I % \$	<H HL DfYZYhWXUV Y 9bUV Y \$
DfYZYhWXUV Y	\$I % (<H HL DfYZYhWXUV Y AUg_ \$
KJ bXckg	\$I %,	<H HL DfYZYhWXUV Y 9bUV Y %
	\$I %7	<H HL DfYZYhWXUV Y AUg_ %
	\$I % \$	<H FL I bWVMXY 9bUV Y \$
	\$I % (<H FL I bWVMXY AUg_ \$
	\$I %,	<H FL I bWVMXY 9bUV Y %
I bWVMXY	\$I %7	<H FL I bWVMXY AUg_ %
KJ bXckg	\$I %5\$	<H FL I bWVMXY 9bUV Y &
	\$I %5(<H FL I bWVMXY AUg_ &
	\$I %5,	<H FL I bWVMXY 9bUV Y '
	\$I %57	<H FL I bWVMXY AUg_ '
	\$I %6\$	<H FL D&D 9bUV Y \$
D&D	\$I %6(<H FL D&D AUg_ \$
KJ bXckg	\$I %6,	<H FL D&D 9bUV Y %
	\$I %67	<H FL D&D AUg_ %

21:0	Reserved	22	0x0		
------	----------	----	-----	--	--

14.5.2 Capability Registers

\$I (\$
 \$I &\$\$%\$\$\$
 7caaUbX 7UdUV]`]h]Yg Dc] bhYf 7UdUV]`]hm =8

14- 9 Command Capabilities Pointer Capability ID

Bit Range	Field Name	Width	Default	Access	Field Description	Field Description
31:29	Slave/Pri	3	0x0	R	Command	HOST/Sec
28:26	Reserved	2	0x0	R		
25:21	Unit Count	5	0x0	R/W		Unit
					<CGH	=8
20:16	Unit ID	5	0x0		G@5J9	l b] h =8
					<CGH#G@5J9	UW\$SUGSg` Uj Y
15:08	Capabilities Pointer	8	0x60	R	Cap	
7:0	Capability ID	8	0x08	R	HyperTransport capability ID	



21 8. 9 6





3C5000L

23	Dw Fc out	1	0x0	R	
22:20	Max Link Width out	3	0x1	R	HT

3C500L

9	Retry Count Rollover	1	0x0	R	Retry
8	Reserved	1	0x0	R	
7:6	Short Retry Attempts	2	0x0	R/W	Short Retry
5:1	Reserved	5	0x0	R	
0	Link Retry Enable	1	0x0	R/W	

14.5.4 Retry Count

<nYfHfUbgdcfh' "\$

\$l , \$\$\$\$\$\$,
 =bhYffi dh 7UdU] `] hm

14- 16 Interrupt Capability

Address	Field Name	Width	Start	Access	Description
31:24	Capabilities Pointer	8	0x80	R	Interrupt discovery and configuration block
23:16	Index	8	0x0	R/W	
15:8	Capabilities Pointer	8	0x0	R	Capabilities Pointer
7:0	Capability ID	8	0x08	R	Hypertransport Capability ID

\$l +(
 \$l \$\$\$\$\$\$\$\$
 8UhUdcf h

14- 17 Dataport

Address	Field Name	Width	Start	Access	Description
31:0	Dataport	32	0x0	R/W	Index 0x10 0xa8 0xac

\$l +,
 \$l : , \$\$\$\$\$\$
 =bhf =bZcO % \$Q

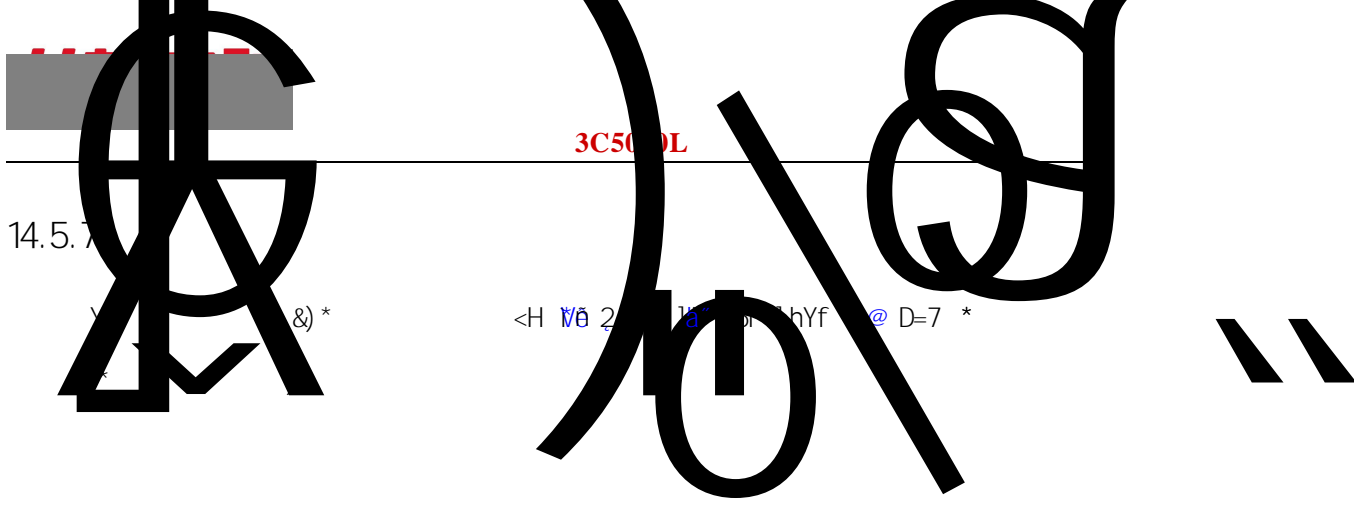
14- 18 IntrInfo 1

Address	Field Name	Width	Start	Access	Description
31:24	IntrInfo[31:24]	8	0xF8	R	
23:2	IntrInfo[23:2]	22	0x0	R/W	IntrInfo[23:2] PIC IntrInfo
1:0	Reserved	2	0x0	R	

\$l +W
 \$l \$\$\$\$\$\$\$\$
 =bhf =bZcO* ' . ' &Q

14- 19 IntrInfo 2

Address	Field Name	Width	Start	Access	Description
31:0	IntrInfo[63:32]	32	0x0	R	



0/ž' ž) ž+ %&+Q % #<H <=)
 0/ž, ž% \$ž% &ž% (&) (Q & #<H <= *
 0/ž- ž% %ž% ' ž%) &) Q ' #<H <= +

\hS] bhSghf] dYS(.

0\$ž (ž, ž%& &) &Q \$ #<H <= (
 0/ž) ž- ž% &) ' Q % #<H <=)
 0&ž *ž%\$ž%(&) (Q & #<H <= *
 0 ž+ž%ž%ž% &) Q ' #<H <= +

\hS] bhSghf] dYS%

\$I, \$
 \$I \$\$\$\$\$\$\$\$
 <H O % \$Q

14- 20 HT 1

31:0	Interrupt_case [31:0]	32	0x0	R/W	HT	[31:0]	0/HTHI	4
------	--------------------------	----	-----	-----	----	--------	--------	---

\$I, (
 \$I \$\$\$\$\$\$\$\$
 <H O' . ' &Q

14- 21 HT 2

31:0	Interrupt_case [63:32]	32	0x0	R/W	HT	[63:32]	0/HTHI	4
------	---------------------------	----	-----	-----	----	---------	--------	---

\$I, ,
 \$I \$\$\$\$\$\$\$\$
 <H O-). *(Q

14- 22 HT 3

--	--	--	--	--	--	--	--	--

3C5000L

Address	Register Name	Width	Reset	Access	Attributes	Range
31:0	Interrupt_case	32	0x0	R/W	HT	[95:64]
	[95:64]					1 /HTHI 5

\$I, W
 \$I \$\$\$\$\$\$\$\$
 <H O%&+. - *Q

14- 23 HT 4

Address	Register Name	Width	Reset	Access	Attributes	Range
31:0	Interrupt_case	32	0x0	R/W	HT	[127:96]
	[127:96]					1 /HTHI 5

\$I - \$
 \$I \$\$\$\$\$\$\$\$
 <H O% - . %&, Q

14- 31 HT 5

Address	Register Name	Width	Reset	Access	Attributes	Range
31:0	Interrupt_case	32	0x0	R/W	HT	[159:128]
	[159:128]					2 /HTHI 6

\$I - (
 \$I \$\$\$\$\$\$\$\$
 <H O% % % \$Q

14- 24 HT 6

Address	Register Name	Width	Reset	Access	Attributes	Range
31:0	Interrupt_case	32	0x0	R/W	HT	[191:160]
	[191:160]					2 /HTHI 6

\$I - ,
 \$I \$\$\$\$\$\$\$\$
 <H O&&' . % &Q

14- 25 HT 7

Address	Register Name	Width	Reset	Access	Attributes	Range
31:0	Interrupt_case	32	0x0	R/W	HT	[223:192]
	[223:192]					3 /HTHI 7

\$I - W



\$! \$\$\$\$\$\$\$

<H

O&). &&(Q

14

\$I U\$
 \$I \$\$\$\$\$\$\$\$
 <H O % \$Q

14- 27 HT 1

31:0	Interrupt_mask [31:0]	32	0x0	R/W	HT	[31:0]	0 /HTH	4
------	--------------------------	----	-----	-----	----	--------	--------	---

\$I U(
 \$I \$\$\$\$\$\$\$\$
 <H O' . ' &Q

14- 28 HT 2

31:0	Interrupt_mask [63:32]	32	0x0	R/W	HT	[63:32]	0 /HTH	4
------	---------------------------	----	-----	-----	----	---------	--------	---

\$I U,
 \$I \$\$\$\$\$\$\$\$
 <H O-). *(Q

14- 29 HT 3

31:0	Interrupt_mask [95:64]	32	0x0	R/W	HT	[95:64]	1 /HTH	5
------	---------------------------	----	-----	-----	----	---------	--------	---

\$I UW
 \$I \$\$\$\$\$\$\$\$
 <H O%&+. - *Q

14- 30 HT 4

31:0	Interrupt_mask [127:96]	32	0x0	R/W	HT	[127:96]	1 /HTH	5
------	----------------------------	----	-----	-----	----	----------	--------	---

\$I V\$



3C5000L

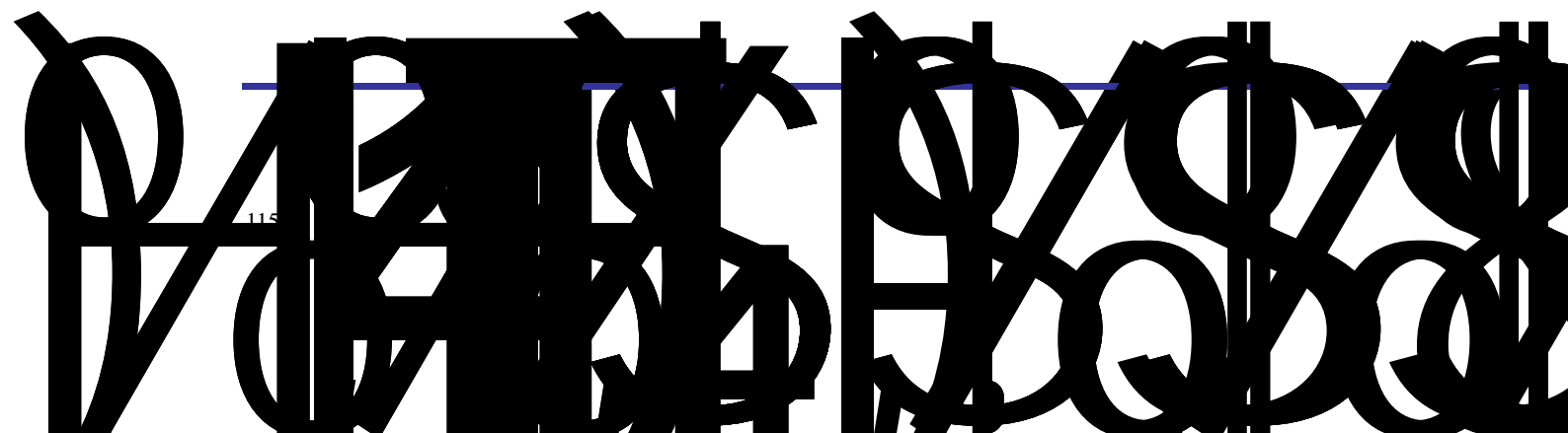
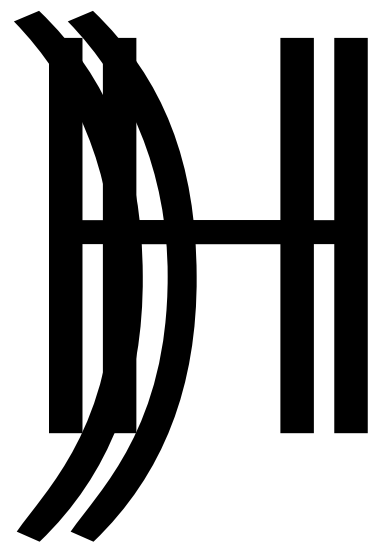
\$! \$\$\$\$\$\$\$\$

<H

0% -. %&, Q

14- 31 HT

5



<H D&D <H D&D
 <H D&D <H 7DI
 D&D <H

\$! % \$
 \$! \$\$\$\$\$\$\$\$
 <H \$

14- 36 HT 0

Bit	Field Name	Width	Reset	Access	Cache	Value	Range
31	ht_rx_image0_en	1	0x0	R/W	HT	0	
30	ht_rx_image0_trans_en	1	0x0	R/W	HT	0	
29	ht_rx_image0_multi_node_en	1	0x0	R/W	HT	0	[39:37] [46:44]
28	ht_rx_image0_conf_hit_en	1	0x0	R/W	HT	0	0
25:0	ht_rx_image0_trans[49:24]	26	0x0	R/W	HT	0	[49:24]

\$! % (
 \$! \$\$\$\$\$\$\$\$
 <H \$

14- 37 HT 0

Bit	Field Name	Width	Reset	Access	Cache	Value	Range
31:16	ht_rx_image0_base[39:24]	16	0x0	R/W	HT	0	[39:24]
15:0	ht_rx_image0_mask[39:24]	16	0x0	R/W	HT	0	[39:24]

\$! % ,
 \$! \$\$\$\$\$\$\$\$
 <H %

14- 38 HT 1

Bit	Field Name	Width	Reset	Access	Cache	Value	Range
31	ht_rx_image1_en	1	0x0	R/W	HT	1	
30	ht_rx_image1_trans_en	1	0x0	R/W	HT	1	

3C5000L

29	ht_rx_image1_multi_node_en	1	Ox0	R/W	HT	1	[39:37] [46:44]
28	ht_rx_image1_conf_hit_en	1	Ox0	R/W	HT	1	0
25:0	ht_rx_image1_trans[49:24]	26	Ox0	R/W	HT	1	[49:24]

\$! % W
 \$! \$\$\$\$\$\$\$\$
 <H %

14- 39 HT 1

31:16	ht_rx_image1_base[39:24]	16	Ox0	R/W	HT	1	[39:24]
15:0	ht_rx_image1_mask[39:24]	16	Ox0	R/W	HT	1	[39:24]

\$! % \$
 \$! \$\$\$\$\$\$\$\$
 <H &

14- 40 HT 2

31	ht_rx_image2_en	1	Ox0	R/W	HT	2	
30	ht_rx_image2_trans_en	1	Ox0	R/W	HT	2	
29	ht_rx_image2_multi_node_en	1	Ox0	R/W	HT	2	[39:37] [46:44]
28	ht						





3C5000L



29	ht_rx_image4_multi_node_en	1	OxO	R/W	HT	4
----	----------------------------	---	-----	-----	----	---

14- 47

30	ht_rx_ext_header_trans_en	1	0x0	R/W	0xFE_00000000 [39:28]
29:0	ht_rx_ext_header_trans[53:24]	30	0x0	R/W	[53:24] [53:29]

14.5.12 POST

%(") " % \$

5L =

5L = 6

DCGH KF =H9

<H

BCBDCGH

KF =H9

<H

<H

5L =

\$! %+\$

\$! \$\$\$\$\$\$\$\$

<H DCGH

\$

14- 48 HT

POST

0

--	--	--	--	--	--

31	ht_post0_en	1	0x0	R/W	HT	POST	0
30	ht_split0_en	1	0x0	R/W	HT	(CPU	uncache
					ACC)	

3C5000L

15:0	ht_post0_mask[39:24]	16	0x0	R/W	HT	POST	0	[39:24]
------	----------------------	----	-----	-----	----	------	---	---------

\$! %+,
 \$! \$\$\$\$\$\$\$\$
 <H DCGH %



14- 50 HT POST 1

31	ht_post1_en	1	0x0	R/W	HT	POST	1	
30	ht_split1_en	1	0x0	R/W	HT	(CPU uncache ACC)		
29:16	Reserved	14	0x0					
15:0	ht_post1_trans[39:24]	16	0x0	R/W	HT	POST	1	[39:24]

\$! %+W
 \$! \$\$\$\$\$\$\$\$
 <H DCGH %

14- 51 HT POST 1

31:16	ht_post1_base[39:24]	16	0x0	R/W	HT	POST	1	[39:24]
15:0	ht_post1_mask[39:24]	16	0x0	R/W	HT	POST	1	[39:24]

14.5.13

%(") " % \$

5L =

757<9

<H

757<9

<H

\$! % \$
 \$! \$\$\$\$\$\$\$\$
 <H \$

3C5000L

31	ht_prefetch0_en	1	0x0	R/W	HT	0	
30:16	Reserved	15	0x0				
15:0	ht_prefetch0_trans[39:24]	16	0x0	R/W	HT	0	[39:24]

\$l % (
 \$l \$\$\$\$\$\$\$\$
 <H \$

14- 53 HT 0

31:16	ht_prefetch0_base[39:24]	16	0x0	R/W	HT	0	[39:24]
15:0	ht_prefetch0_mask[39:24]	16	0x0	R/W	HT	0	[39:24]

\$l % ,
 \$l \$\$\$\$\$\$\$\$
 <H %

14- 54 HT 1 b



<H

G757<9

757<9

=C 757<9

757<9

3C5000L

30	ht_uncache1_trans_en	1	0x0	R/W	HT	uncache	1
29	ht_uncache1_multi_node_en	1	0x0	R/W	HT	uncache	1
28	ht_uncache1_conf_hit_en	1	0x0	R/W	HT	uncache	1
25:0	ht_uncache1_trans[49:24]	26	0x0	R/W	HT	uncache [49:24]	1



3C5000L

14- 61 HT Uncache 2

[Redacted Header]								
31:16	ht_uncache2_base[39:24]	16	0x0	R/W	HT	uncache	2	[39:24]
15:0	ht_uncache2_mask[39:24]	16	0x0	R/W	HT	uncache	2	[39:24]

3C5000L

\$l %6\$
 \$l \$\$\$\$\$\$\$\$
 <H D&D \$

14- 64 HT P2P 0

31	ht_rx_p2p0_en	1	0x0	R/W	HT	P2P	0	
29:0	ht_rx_p2p0_trans[53:24]	30	0x0	R/W	HT	P2P	0	[53:24]

\$l %6(
 \$l \$\$\$\$\$\$\$\$
 <H D&D \$

14- 65 HT P2P 0

31:16	ht_rx_p2p0_base[39:24]	16	0x0	R/W	HT	P2P	1	[39:24]
15:0	ht_rx_p2p0_mask[39:24]	16	0x0	R/W	HT	P2P	1	[39:24]



14.5.16

\$! %/\$

\$! \$\$- \$(' &%

5DD 7CB: =; \$

14- 68

3C5000L

					0xF
--	--	--	--	--	-----

\$! %7(
 \$! \$\$- \$(' &%
 5DD 7CB: =; %

14- 69

1

31	tx post split en	1	0x0	R/W	hl dcgh =8 ' & VmhY kf] hY
30	tx wr passPW pc	1	0x0	R/W	Dcgh dUggDK %
29	tx wr passPW npc	1	0x0	R/W	Bcbdcgh dUggDK %
28	tx rd passPW	1	0x0	R/W	dUggDK %
27	stop same id wr	1	0x0	R/W	5L= =8 =8
26	stop same id rd	1	0x0	R/W	5L= =8 =8
25	Not axi2seqid wr	1	0x0	R/W	5L= =8 gYe] X Z]I YX gYe] X
24	Not axi2seqid rd	1	0x0	R/W	5L= =8 gYe] X Z]I YX gYe] X
23:22	Reserved	2	0x0	R/W	
21	act as slave	1	0x1	R/W	G@5J9
20	Host hide	1	0x0	R/W	
19:16	Rrequest delay	4	0x3	R/W	Rrequest 000 0 001 0-8 010 8-15 011 16-31 100 32-63 101 64-127 110 128-255 111 0



3C5000L

15	Crc Int en	1	0x0	R/W	7F7
14:12	Crc Int route	3	0x0	R/W	7F7
11	Reserved				
10	ht int 8 bit	1	0x0	R/W	, 3
9:8	ht_int_stripe	2	0x0	R/W	0x0 ht_int_stripe_1 0x1 ht_int_stripe_2 0x2 ht_int_stripe_4
4:0	Interrupt Index	5	0x0	R/W	

14.5.18 PHY

D<M

\$! %77

\$! , ' ' \$, \$\$\$

D<M

14- 71 PHY

31:29	Reserved	3	0x0	R	
28	dll locked hi	1	0x0	R	, 8@@
27	dll locked lo	1	0x0	R	, 8@@
26	cdr locked hi	1	0x0	R	, 78F
25	cdr locked lo	1	0x0	R	, 78F
24	phase locked	1	0x0		

14.5.20

\$! %8(
\$! \$\$\$\$\$\$\$\$

14- 73

31	Reserved	1	0x0	R	
30	rx_buffer_r_data[4]	1	0x0	R/W	buffer V] hQ Q
29	rx_buffer_npc_data[4]	1	0x0	R/W	npc buffer V] hQ Q
28	rx_buffer_pc_data[4]	1	0x0	R/W	pc buffer V] hQ Q
27	rx_buffer_b_cmd[4]	1	0x0	R/W	bresponse buffer V] hQ Q
26	rx_buffer_r_cmd[4]	1	0x0	R/W	buffer V] hQ Q
25	rx_buffer_npc_cmd[4]	1	0x0	R/W	npc buffer V] hQ Q
24	rx_buffer_pc_cmd[4]	1	0x0	R/W	pc buffer V] hQ Q
23:16	R_DATA_txbuffer	8	0x0	R	R
15:8	NPC_DATA_txbuffer	8	0x0	R	NPC
7:0	PC_DATA_txbuffer	8	0x0	R	PC

14.5.21

<H

\$! %8,
\$! \$\$\$\$\$\$\$\$

14- 74

--	--	--	--	--	--

31	b_interleave	1	0	R/W	6
30	nop_interleave	1	0	R/W	
29	Tx_neg	1	0	R/W	0 1 +1
28	Tx_buff_adj_en	1	0x0	R/W	0->1
27:24	R_DATA_txadj	4	0x0	R/W	R tx_neg 0 R_DATA_txadj tx_neg 1 R_DATA_txadj+1
23:20	NPC_DATA_txadj	4	0x0	R/W	NPC tx_neg 0 NPC_DATA_txadj tx_neg 1 NPC_DATA_txadj+1
19:16	PC_DATA_txadj	4	0x0	R/W	PC tx_neg 0 PC_DATA_txadj tx_neg 1 PC_DATA_txadj+1
15:12	B_CMD_txadj	4	0x0	R/W	B tx_neg 0 B_CMD_txadj tx_neg 1 B_CMD_txadj+1
11:8	R_CMD_txadj	4	0x0	R/W	R tx_neg 0 R_CMD_txadj tx_neg 1 R_CMD_txadj+1
7:4	NPC_CMD_txadj	4	0x0	R/W	NPC / tx_neg 0 NPC_CMD_txadj tx_neg 1 NPC_CMD_txadj+1
3:0	PC_CMD_txadj	4	0x0	R/W	PC tx_neg 0 PC_CMD_txadj tx_neg 1 PC_CMD_txadj+1

14.5.22

\$I

14- 75

27:24	rx_buffer_r_data	4	0x0	R/W	buffer
23:20	rx_buffer_npc_data	4	0x0	R/W	npc buffer
19:16	rx_buffer_pc_data	4	0x0	R/W	pc buffer
15:12	rx_buffer_b_cmd	4	0x0	R/W	bresponse buffer
11:8	rx_buffer_r_cmd	4	0x0	R/W	buffer
7:4	rx_buffer_npc_cmd	4	0x0	R/W	npc buffer
3:0	rx_buffer_pc_cmd	4	0x0	R/W	pc buffer

14.5.23 Training 0

```

<mYfHfUbgdcf h' "$      HfU] b] b[ $
<mdYfHfUbgdcf h' "$      %#(
    $! %Ø$
    $! $$$$$$, $
    HfU] b] b[ $

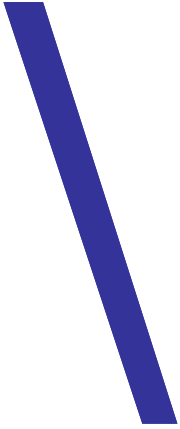
```

14- 76 Training 0





3C5000L





3C500L

T3 til	32	0x7ffff	R/W	Training 3
--------	----	---------	-----	------------

14.5.28

D@@

%

D@@

X]j SfYZW X]j S' ccd ž

d\ns\] SX]j d\ns` cSX]j

VtfYSX]j

kUfa

fYgYh @8H X]gVtbbYVh

D@@

D<M\$@=B?S7@? <H

GMS7@C7? ?



\$! \$\$\$\$\$\$\$\$

14- 81



31	27	PLLrelock counter	5	0x0	R/W		Wti bhYf
----	----	-------------------	---	-----	-----	--	----------

gY` YWñ

oD@sfY` cW_SWti bhYf ž) \%Zq

;% ' ZZ

26	Counter select	1	0x0	R/W
----	----------------	---	-----	-----

% V\$

% V% D@sfY` f Dfc ñ`





3C5000L

16:12	Tx_preenmp	5	0x08	R/W	PAD
11 0	Reserved	12	0x0	R	

14.5.31

```

                <mdYfHfUbgdcfh ' "$
                D<M      78F
`cW_          78F
                78F

                $! &($
                $! $$$$$$$$

```

14- 84



15 Cdr_ignore_enable 1 0x0 R/W



3C5000L

14- 90 LDT

5



3C5000L

15:0	HT TX POST ID2 BASE	16	0x0	R/W	5L= =8	DCGH
						=8 65G9

\$! &*7
 \$! \$\$\$\$\$\$\$\$
 <H HL DCGH =8 K=B'

14- 94 HT TX POST ID WIN3

31:16	HT TX POST ID3 MASK	16	0x0	R/W	5L= =8	DCGH
						=8 A5G?
15:0	HT TX POST ID3 BASE	16	0x0	R/W	5L= =8	DCGH
						=8 65G9

14.5.34

<H =C
 <H =C

\$! &+\$
 \$! \$\$\$\$\$\$\$\$
 <H FL =BH HF5BG @c

14- 95 HT RX INT TRANS LO

31:4	INT_trans_addr[31:4]	28	0x0	R/W	
3:0	Reserved	4	0x0	R	

\$! &+(
 \$! \$\$\$\$\$\$\$\$
 <H FL =BH HF5BG <]

14- 96 HT RX INT TRANS Hi

31	INT_trans_en	1	0x0	R/W	
30	INT_trans_allow	1	0x0	R/W	=BhShf UbgSYb 9LHs=BhSYb



3C5000L

29:26	INT_trans_cache	4	0x0	R/W	7UWY
25:0	INT_trans_addr[57:32]	26	0x0	R/W	

14.6 HyperTransport

<mYf Hf Ubgdcf h

D7=

% - *

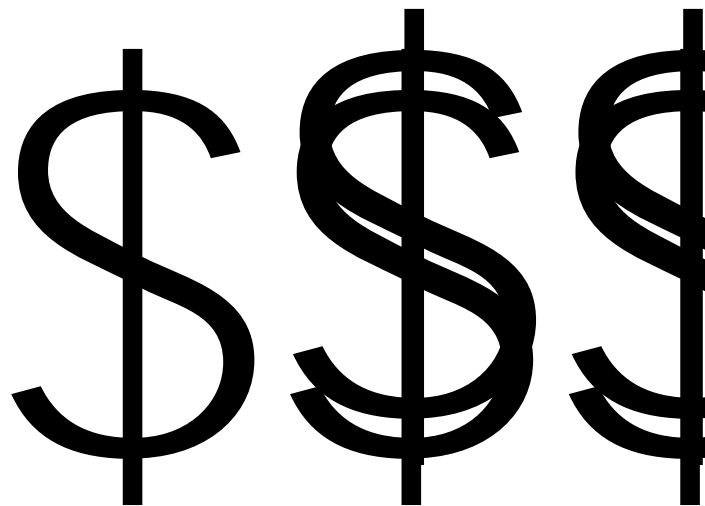
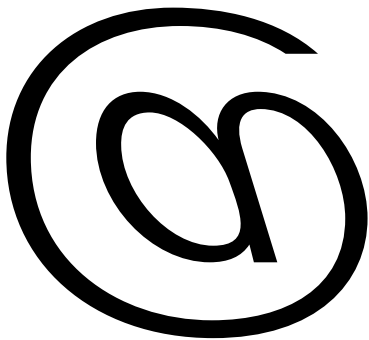
<H

\$l : 8S: 9\$\$\$\$\$\$\$

\$l : 8S: ::: S: :::

<H

' 7) \$\$\$@



15

IO



' =#C I 5FH GD= =&7 ; D=C =#C
5L= 7DI

15.1 UART

I 5FH
' /
'
' 16
'
'
' FIFO
' NS16550A
'
' H a "



15.1.2

IER

[7 0]

0x01

0x00



7:4	Reserved	4	RW		
3	IME	1	RW	Modem	'0' – '1' –

Б ! 0° E) ..

9^

+4' to 'E

0	1	1	1st			LSR
0	1	0	2nd		FIFO trigger	FIFO trigger
1	1	0	2nd		FIFO 4	FIFO
		0	3rd			THR IIR
0	0	0	4th	Modem	CTS, DSR, RI or DCD.	MSR

15.1.4 FIFO

FCR

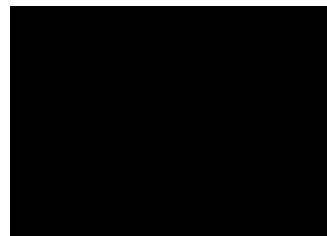
FIFO
[7 0]
0x02
0xc0

>D89BXΓ•Π



7:6

rr



B+8

μ:θθ

r

o



3C5000L

3	pe	1	RW	'0' – '1' –
2	sb	1	RW	'0' – 1 '1' – 5 1.5 2
1:0	bec	2	RW	'00' – 5 '01' – 6 '10' – 7 '11' – 8

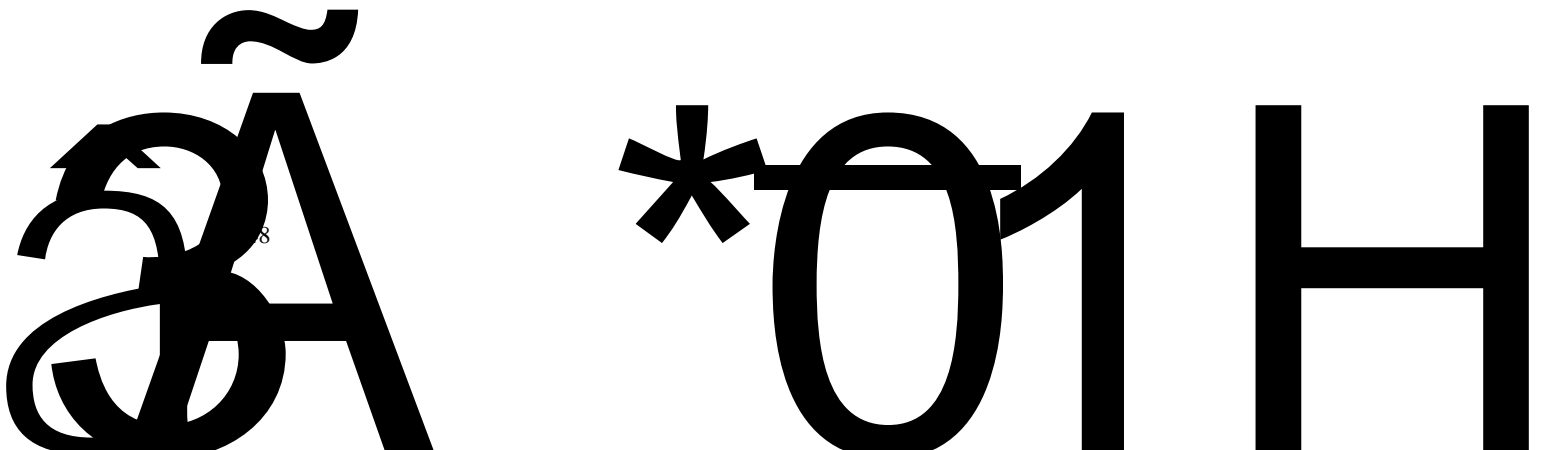
h

15.1.6 MODEM

MCR

Modem

[7 0]





3C5000L



DTR è DSR

RTS è CTS

Out1 è RI

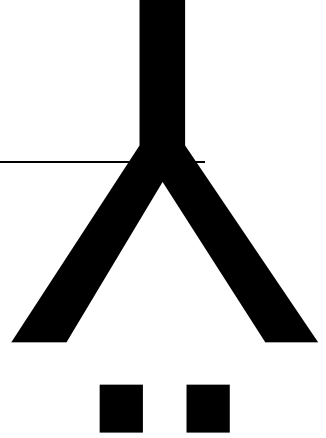
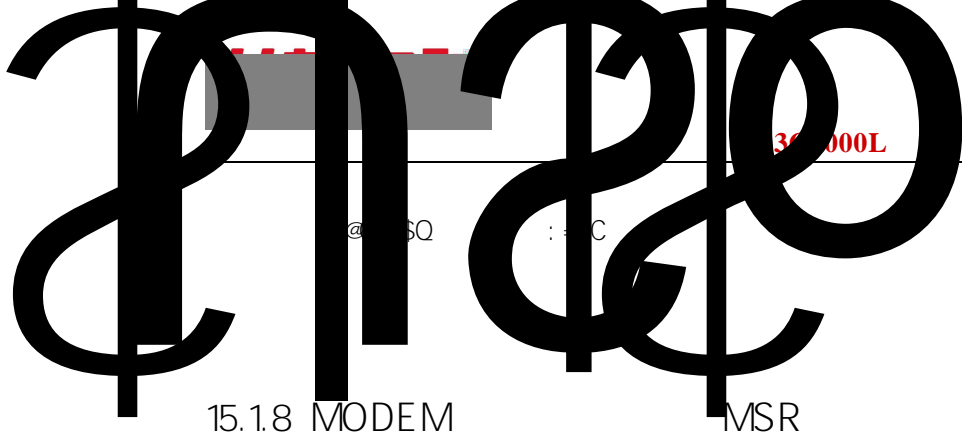
Out2 è DCD

3	OUT2	1	W		DCD
2	OUT1	1	W		RI
1	RTSC	1	W	RTS	fz

b



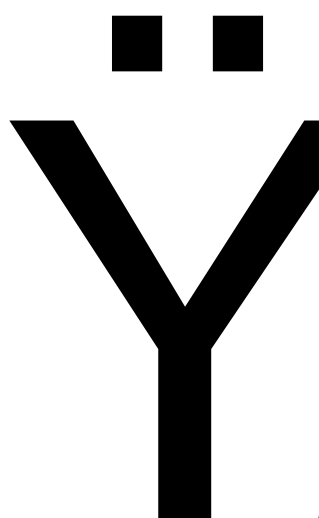
3C5000L



Modem
[7 0]
0x06

AG 6, T
(B) 0B
L

OM



3C5000L

0x00

7:0	D_DIV	8	RW	

15.1.12

: =: C F: 7 7DI : =: C 7DI

7DI I 5FH

: =: C H: 7 7DI : =: C 7DI

: =: C 7DI I 5FH

,

%%\$A<n %*

AG6 @G6 &)* 8S8=J

15.2 SPI

GD=

,

,

GD= \$! % 9\$\$\$ \$

15- 1 SPI

SPI Boot	0X1FC0_0000-0X1FD0_0000	1MByte
SPI Memory	0X1D00_0000-0X1E00_0000	16MByte
SPI Register	0X1FE0_01F0-0X1FE0_01FF	16Byte

GD= 6cch \$! 6: 7\$\$\$\$\$

GD=

GD= AYacfm

7DI

GD= 6CCH

15.2.1

SPCR

[7 0]



15.2.2

SPSR



15.2.4

SPER

[7 0]

0x03

0x00



0	memory_en	1	RW	spi flash	csn[0]
---	-----------	---	----	-----------	--------

15.2.6 SFC_SOFTCS

SPI Flash

[7 0]

0x05

0x00

SFC_SOFTCS					
7:4	csn	4	RW	csn	
3:0	csen	4	RW	1	cs 7:4

15.2.7 SFC_TIMING

SPI Flash

[7 0]

0x06

0x03

SFC_TIMING					
7:4	Reserved	4	RW		
3	quad_io	1	RW	4	1
2	tFast	1	RW		
1:0	tCSH	2	RW	SPI Flash T 00: 1T 01: 2T 10: 4T 11: 8T	

15.2.8

CTRL

SPI Flash

[7 0]

0x08

0x00

7:4	nbyte	4	RW	
3:2	reserve	2	RW	
1	nbmode	1	RW	
0	start	1	RW	

15.2.9

CMD

SPI Flash

[7 0]

0x09

0x00

7:0	cmd	8	RW	spi flash

15.2.10

0 BUFO

SPI Flash

0

[7 0]

0x0a

0x00

7:0	buf0	8	RW	SPI SPI





: @5G<

15.3 I2C

=&7

=&7

=&7

G85

G7@

(\$\$_Vdg

' 7) \$\$\$@

=&7

G@S7HF@O*. \$Q

=&7\$

\$I % 9\$\$%&\$

=&7%

\$I % 9\$\$% \$

15.3.1

PRERlo

[7 0]

0x00

0xff

7:0	PRERlo	8	RW	8
-----	--------	---	----	---

15.3.2

PRERhi

[7 0]

0x01

0xff

7:0	PRERhi	8	RW	8
-----	--------	---	----	---

dfYgWU` Y @D6 D7@? WcW_SUG7@

WcW_Sg

DfWgWU` Y 1 WcW_SU#f(! WcW_Sg! %

15.3.3 CTR

[7 0]

0x02

0x20

7	EN	1	RW	1 , 0
6	IEN	1	RW	1
5	MST_EN	1	RW	0 slave 1 master
4:0	Reserved	5	RW	

15.3.4 TXR

[7 0]

0x03

0x00

7:1	DATA	7	W	
0	DRW	1	W	



15.3.5

3C5000L

				0
6	Busy	1	R	I2c 1 0
5	AL	1	R	I2C I2C 1
4:2	Reserved	3	R	
1	TIP	1	R	1 0
0	IF	1	R	1

15.3.8

SLV_CTRL

[7 0]

0x07

0x00

7	SLV_EN	1	WR	MST_EN 0
6 0	SLV_ADDR	7	WR	I2C